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ACL Data Book

1987

Advanced CMOS Logic



TEXAS
INSTRUMENTS

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Advanced CMOS Circuits

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Advanced CMOS Logic Data Book

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Advanced CMOS Logic Data Book

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INTRODUCTION

Benefits of the 1-micron EPIC™ Advanced CMOS Logic (ACL) family (54/74AC/ACT11XXX) from Texas Instruments include:

- Advanced bipolar propagation delays
- Low CMOS power consumption
- 24-mA output drive
- Significant reduction in output voltage noise

Featuring both CMOS- (AC) and TTL- (ACT) compatible functions, the new devices can enhance the performance of high-speed CMOS designs or reduce power requirements in advanced bipolar designs without sacrificing the advantages of either technology.

EPIC™ ACL ensures reliable system operation by reducing simultaneous switching noise, voltage noise generated when multiple outputs are switched. A function of package inductance and the rate of change in current (di/dt), switching noise is of greater concern for ACL than for bipolar designs because of the wider swings of CMOS transistors.

Because the "end-pin" location of power and ground maximizes package inductance, conventionally-packaged ACL creates noise spikes that can lead to the loss of stored data, output glitching, and performance degradation. To ensure system reliability, the designer is forced to use noise-control techniques that detract from system performance, such as adding series resistors to device outputs.

In EPIC™ ACL, power and ground pins have been assigned to package-center to reduce overall package inductance. Combined with a new circuit design technique called OEC™ (Output Edge Control), which softens the edges of the output wave without compromising overall speed, center-pin packaging significantly reduces system-level noise.

TI's EPIC™ ACL family provides the following:

- 50% noise level reduction over end-pin ACL; 10% reduction over advanced bipolar devices
- Flow-through architecture that simplifies design
- Lower design cost due to lower parts count (no space sacrificed to passive components)
- A broad range of over 100 planned functions
- Co-development with Philips/Signetics.

This data book presents pertinent technical information on available EPIC™ ACL devices. In addition, the General Information section contains a functional index of all EPIC™ ACL devices, available or under development, as well as device pinout information for the entire EPIC™ ACL family.

Further information on TI's EPIC™ ACL and other semiconductor products is available from your nearest TI field sales office, local authorized distributor, or by calling Texas Instruments at 1-800-232-3200.

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54ACT11004	74ACT11004	†	1-27
54AC11008	74AC11008	2-19	1-27
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54ACT11010	74ACT11010	2-31	1-27
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54ACT11032	74ACT11032	2-79	1-28
54AC11034	74AC11034	†	1-28
54ACT11034	74ACT11034	†	1-28
54AC11074	74AC11074	2-83	1-28
54ACT11074	74ACT11074	2-89	1-28
54AC11109	74AC11109	2-93	1-28
54ACT11109	74ACT11109	2-99	1-28
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54ACT11112	74ACT11112	†	1-28
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†For more information on these devices, contact the factory.

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54AC11174	74ACT11174	1-30
54ACT11174	74ACT11174	1-30
54AC11175	74ACT11175	1-30
54ACT11175	74ACT11175	1-30
54AC11181	74ACT11181	1-30
54ACT11181	74ACT11181	1-30
54AC11190	74ACT11190	1-30
54ACT11190	74ACT11190	1-30
54AC11191	74ACT11191	1-30
54ACT11191	74ACT11191	1-30
54AC11192	74ACT11192	1-30
54ACT11192	74ACT11192	1-30
54AC11193	74ACT11193	1-31
54ACT11193	74ACT11193	1-31
54AC11194	74ACT11194	1-31
54ACT11194	74ACT11194	1-31
54AC11238	74ACT11238	1-31
54ACT11238	74ACT11238	1-31
54AC11239	74ACT11239	1-31
54ACT11239	74ACT11239	1-31
54AC11240	74ACT11240	2-103
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54ACT11241	74ACT11241	2-119
54AC11244	74ACT11244	2-123
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54AC11245	74ACT11245	2-133
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54AC11251	74ACT11251	1-31
54ACT11251	74ACT11251	1-31
54AC11253	74ACT11253	1-32
54ACT11253	74ACT11253	1-32
54AC11257	74ACT11257	1-32
54ACT11257	74ACT11257	1-32
54AC11258	74ACT11258	1-32
54ACT11258	74ACT11258	1-32
54AC11269	74ACT11269	1-32
54ACT11269	74ACT11269	1-32
54AC11280	74ACT11280	1-32
54ACT11280	74ACT11280	1-32
54AC11286	74ACT11286	1-32
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[†]For more information on these devices, contact the factory.

For more information on these devices, contact the factory.

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54ACT11373 74ACT11373	2-149	1-33
54AC11374 74AC11374	2-155	1-33
54ACT11374 74ACT11374	2-161	1-33
54AC11378 74AC11378	†	1-33
54ACT11378 74ACT11378	†	1-33
54AC11379 74AC11379	†	1-33
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54AC11521 74AC11521	2-176	1-33
54ACT11521 74ACT11521	2-180	1-33
54AC11533 74AC11533	2-184	1-33
54ACT11533 74ACT11533	2-189	1-33
54AC11534 74AC11534	2-195	1-33
54ACT11534 74ACT11534	2-201	1-33
54AC11568 74AC11568	†	1-34
54ACT11568 74ACT11568	†	1-34
54AC11569 74AC11569	†	1-34
54ACT11569 74ACT11569	†	1-34
54AC11579 74AC11579	†	1-34
54ACT11579 74ACT11579	†	1-34
54AC11620 74AC11620	2-207	1-34
54ACT11620 74ACT11620	2-213	1-34
54AC11623 74AC11623	2-219	1-34
54ACT11623 74ACT11623	2-225	1-34
54AC11640 74AC11640	2-231	1-34
54ACT11640 74ACT11640	2-237	1-34
54AC11643 74AC11643	2-241	1-34
54ACT11643 74ACT11643	2-247	1-34
54AC11646 74AC11646	2-251	1-34
54ACT11646 74ACT11646	2-259	1-34
54AC11648 74AC11648	†	1-34
54ACT11648 74ACT11648	†	1-34
54AC11651 74AC11651	†	1-35
54ACT11651 74ACT11651	†	1-35
54AC11652 74AC11652	†	1-35
54ACT11652 74ACT11652	†	1-35
54AC11657 74AC11657	†	1-35
54ACT11657 74ACT11657	†	1-35
54AC11818 74AC11818	†	1-35
54ACT11818 74ACT11818	†	1-35
54AC11819 74AC11819	†	1-35
54ACT11819 74ACT11819	†	1-35
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†For more information on these devices, contact the factory.

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54ACT11826	74ACT11826	1-36
54AC11827	74AC11827	1-36
54ACT11827	74ACT11827	1-36
54AC11828	74AC11828	1-37
54ACT11828	74ACT11828	1-37
54AC11833	74AC11833	1-37
54ACT11833	74ACT11833	1-37
54AC11834	74AC11834	1-37
54ACT11834	74ACT11834	1-37
54AC11841	74AC11841	1-37
54ACT11841	74ACT11841	1-37
54AC11842	74AC11842	1-37
54ACT11842	74ACT11842	1-37
54AC11843	74AC11843	1-37
54ACT11843	74ACT11843	1-37
54AC11844	74AC11844	1-38
54ACT11844	74ACT11844	1-38
54AC11845	74AC11845	1-38
54ACT11845	74ACT11845	1-38
54AC11846	74AC11846	1-38
54ACT11846	74ACT11846	1-38
54AC11853	74AC11853	1-38
54ACT11853	74ACT11853	1-38
54AC11854	74AC11854	1-38
54ACT11854	74ACT11854	1-38
54AC11861	74AC11861	1-38
54ACT11861	74ACT11861	1-38
54AC11862	74AC11862	1-39
54ACT11862	74ACT11862	1-39
54AC11863	74AC11863	1-39
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54AC11864	74AC11864	1-39
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54AC11874	74AC11874	1-39
54ACT11874	74ACT11874	1-39
54AC11881	74AC11881	1-39
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†For more information on these devices, contact the factory.

†For more information on these devices, contact the factory.

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

C_i	Input capacitance The internal capacitance at an input of the device.
C_o	Output capacitance The internal capacitance at an output of the device.
C_{pd}	Power dissipation capacitance Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$
f_{max}	Maximum clock frequency The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.
I_{CC}	Supply current The current into* the V _{CC} supply terminal of an integrated circuit.
ΔI_{CC}	Supply current change (ACT devices only) The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V _{CC} .
I_{IH}	High-level input current The current into* an input when a high-level voltage is applied to that input.
I_{IL}	Low-level input current The current into* an input when a low-level voltage is applied to that input.
I_{OH}	High-level output current The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.
I_{OL}	Low-level output current The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.
I_{OZ}	Off-state (high-impedance-state) output current (of a three-state output) The current flowing into* an output having three-state capability with input conditions established that, according to the production specification, will establish the high-impedance state at the output.

*Current out of a terminal is given as a negative value.

GLOSSARY SYMBOLS, TERMS, AND DEFINITIONS

1 General Information

t_a	Access time The time interval between the application of a specified input pulse and the availability of valid signals at an output.
t_{dis}	Disable time (of a three-state or open-collector output) The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state. NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ} . Open-collector outputs will change only if they are low at the time of disabling so $t_{dis} = t_{PLH}$.
t_{en}	Enable time (of a three-state or open-collector output) The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low). NOTE: In the case of memories, this is the access time from an enable input (e.g., \bar{G}). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL} . Open-collector outputs will change only if they are responding to data that would cause the output to go low so, for them, $t_{en} = t_{PHL}$.
t_h	Hold time The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal. NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed. 2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.
t_{pd}	Propagation delay time The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. ($t_{pd} = t_{PHL}$ or t_{PLH}).
t_{PHL}	Propagation delay time, high-to-low level output The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.
t_{PHZ}	Disable time (of a three-state output) from high level The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.
t_{PLH}	Propagation delay time, low-to-high-level output The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.
t_{PLZ}	Disable time (of a three-state output) from low level The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.
t_{PZH}	Enable time (of a three-state output) to high level The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL}	<p>Enable time (of a three-state output) to low level</p> <p>The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.</p>
t_{su}	<p>Setup time</p> <p>The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.</p> <p>NOTES:</p> <ol style="list-style-type: none"> 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed. 2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.
t_w	<p>Pulse duration (width)</p> <p>The time interval between specified reference points on the leading and trailing edges of the pulse waveform.</p>
V_{IH}	<p>High-level input voltage</p> <p>An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.</p> <p>NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.</p>
V_{IL}	<p>Low-level input voltage</p> <p>An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.</p> <p>NOTE: A minimum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.</p>
V_{OH}	<p>High-level output voltage</p> <p>The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.</p>
V_{OL}	<p>Low-level output voltage</p> <p>The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.</p>
V_{T+}	<p>Positive-going threshold level</p> <p>The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.</p>
V_{T-}	<p>Negative-going threshold level</p> <p>The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.</p>



EXPLANATION OF FUNCTION TABLES

SYMBOLS, TERMS, AND DEFINITIONS



1

General Information

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
↕	=	value/level or resulting value/level is routed to indicated destination
↺	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a . . h	=	the level of steady-state inputs at inputs A through H respectively
Q ₀	=	level of Q before the indicated steady-state input conditions were established
\bar{Q}_0	=	complement of Q ₀ or level of \bar{Q} before the indicated steady-state input conditions were established
Q _n	=	level of Q before the most recent active transition indicated by ↓ or ↑
	=	one high-level pulse
	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q₀, or \bar{Q}_0), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse,  or , the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

FUNCTION TABLE													
INPUTS							OUTPUTS						
CLEAR	MODE		CLOCK	SERIAL		PARALLEL			Q _A	Q _B	Q _C	Q _D	
	S1	S0		LEFT	RIGHT	A	B	C					D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}
H	H	L	↑	H	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

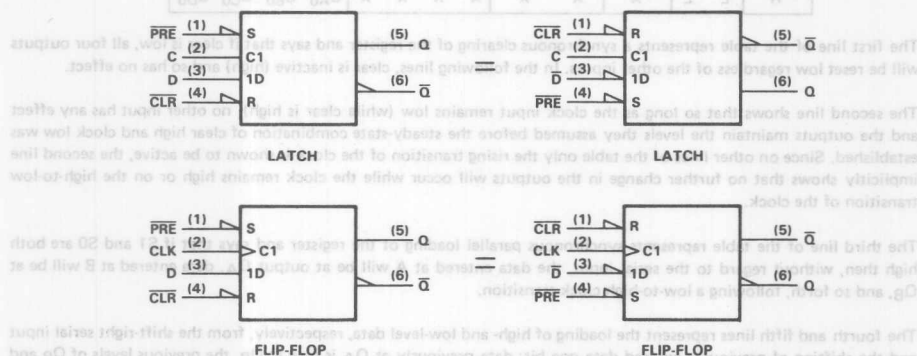
The function table functional tests do not reflect all possible combinations or sequential modes.

D flip-flop and latch signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called \bar{Q} . An input that causes a Q output to go high or a \bar{Q} output to go low is called Preset (PRE). An input that causes a \bar{Q} output to go high or a Q output to go low is called Clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active-low.

The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits \bar{D} and Q.

In some applications, it may be advantageous to redesignate the data input from D to \bar{D} or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown in parentheses.



The figures show that when Q and \bar{Q} exchange names, the Preset and Clear pins also exchange names. The polarity indicators (∇) on \bar{PRE} and \bar{CLR} remain, as these inputs are still active-low, but the presence or absence of the polarity indicator changes at D (or \bar{D}), Q, and \bar{Q} . Pin 5 (Q or \bar{Q}) is still in phase with the data input (D or \bar{D}); their active levels change together.

In digital system design, consideration must be given to thermal management of components. The small size of the "small outline" package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the EPIC™ ACL family. In general, the junction temperature for any device can be calculated using Equation 1.

$$T_J = R_{\theta JA} \times P_T + T_A \quad (1)$$

where

T_J = virtual junction temperature
 $R_{\theta JA}$ = thermal resistance, junction to free air
 P_T = total power dissipation of the device
 T_A = free-air temperature

The total power consumption can be determined from Equation 2 for an AC device and Equation 3 for an ACT device.

$$P_T = V_{CC} \times I_{CC} + (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma (C_L \times V_{CC}^2 \times f_o) \quad (2)$$

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} + d_c)] + (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma (C_L \times V_{CC}^2 \times f_o) \quad (3)$$

where

V_{CC} = supply voltage (5 V for typical, 5.5 V for maximum) see Note 1
 I_{CC} = quiescent supply current (specified on device data sheet)
 C_{pd} = Power dissipation capacitance (from the device data sheet)
 f_i = input frequency
 C_L = output load capacitance
 f_o = output frequency
 N = number of inputs driven by a TTL device
 d_c = duty cycle
 ΔI_{CC} = increase in supply current (specified on device data sheet)

NOTE 1: In system applications I_{CC} can be minimized by keeping input voltage levels less than 1 V for V_{IL} and greater than $V_{CC} - 1$ V for V_{IH} and input rise and fall times less than 15 ns.

JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
AIR VELOCITY

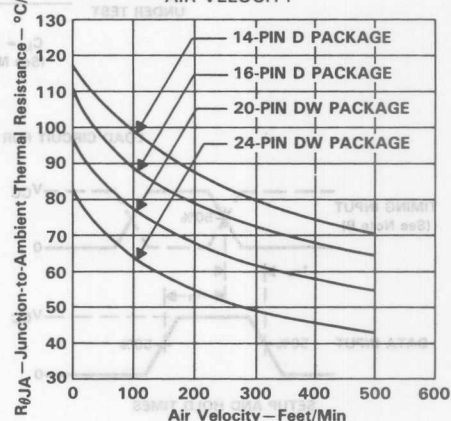


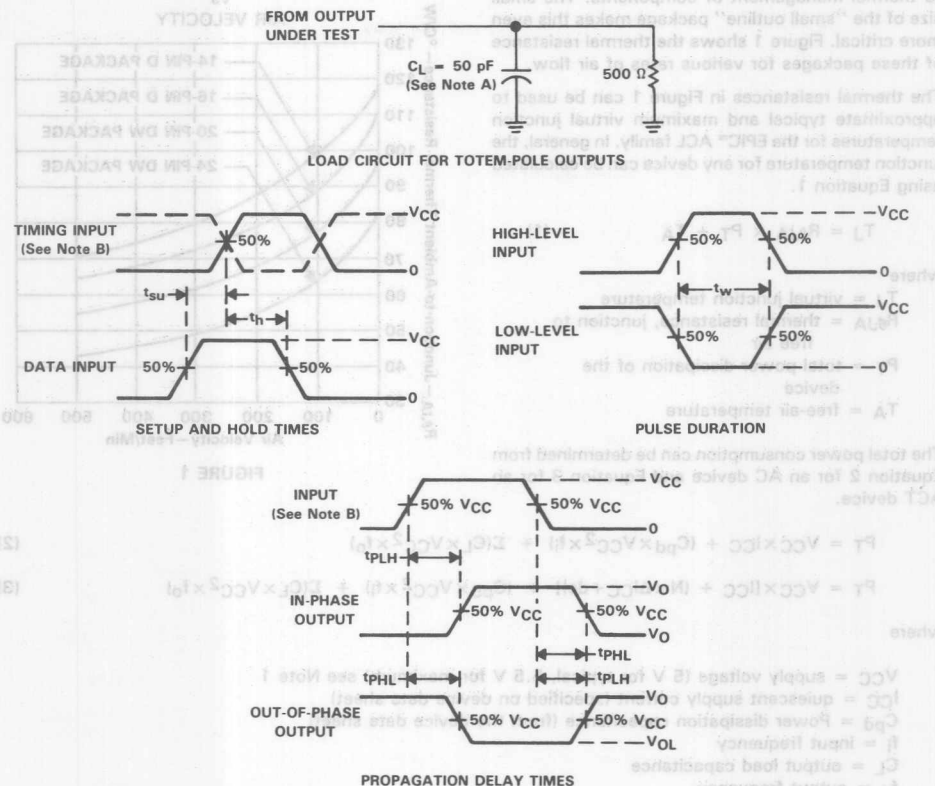
FIGURE 1

PARAMETER MEASUREMENT INFORMATION

1

General Information

SERIES 54AC11XXX AND 74AC11XXX DEVICES



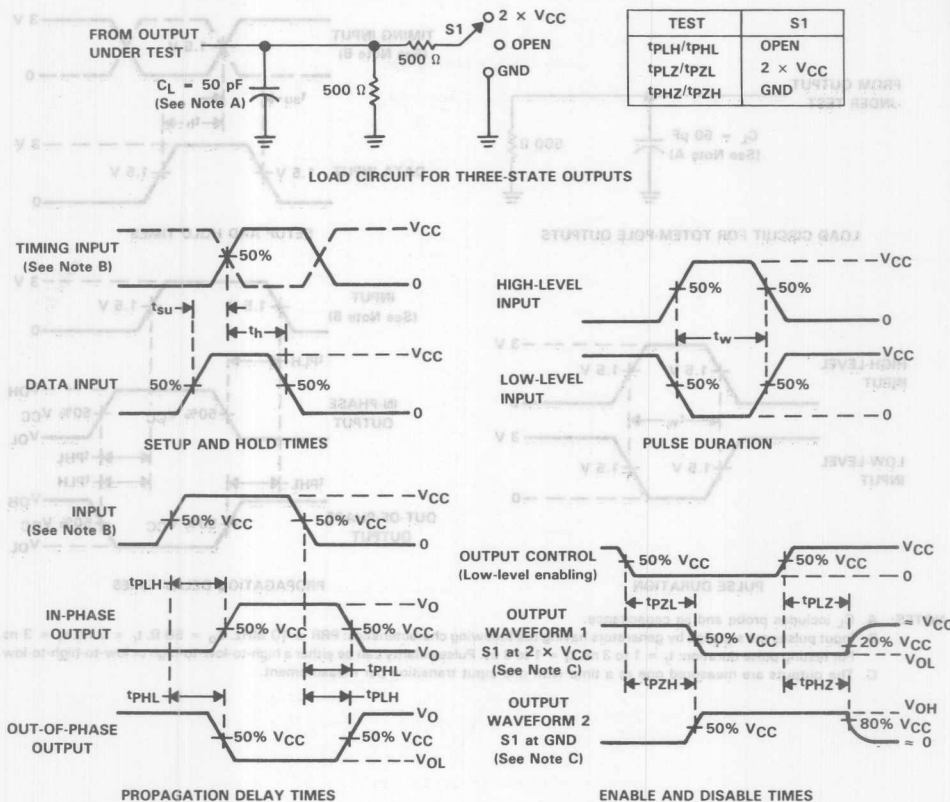
NOTES: A. C_L includes probe and jig capacitance.

B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_0 = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.

For testing pulse duration: $t_r = 1 \text{ to } 3 \text{ ns}$, $t_f = 1 \text{ to } 3 \text{ ns}$. Pulse polarity can be either a high-to-low-to-high or low-to-high-to-low.

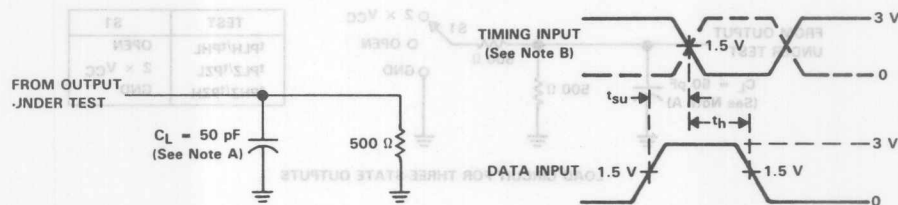
C. The outputs are measured one at a time with one input transition per measurement.

SERIES 54AC11XXX AND 74AC11XXX DEVICES

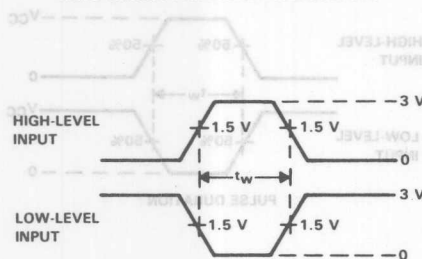


- NOTES: A. C_L includes probe and jig capacitance.
- B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_0 = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns. For testing pulse duration: $t_r = 1$ to 3 ns, $t_f = 1$ to 3 ns. Pulse polarity can be either a high-to-low-to-high or low-to-high-to-low.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one input transition per measurement.

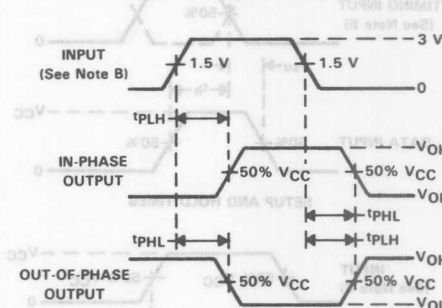
SERIES 54ACT11XXX AND 74ACT11XXX DEVICES



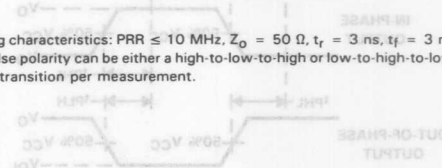
LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS



SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES



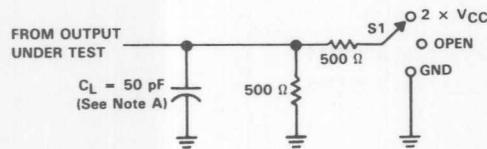
NOTES: A. C_L includes probe and jig capacitance.

B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.

For testing pulse duration: $t_r = 1$ to 3 ns, $t_f = 1$ to 3 ns. Pulse polarity can be either a high-to-low-to-high or low-to-high-to-low.

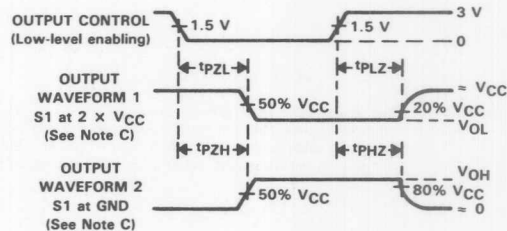
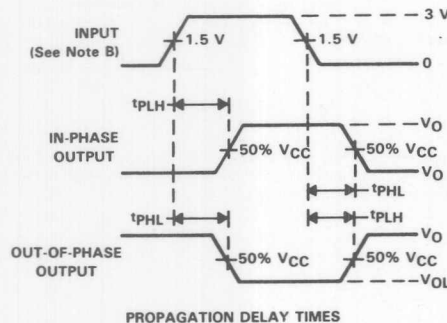
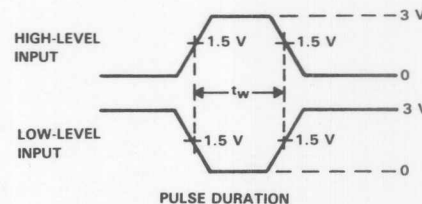
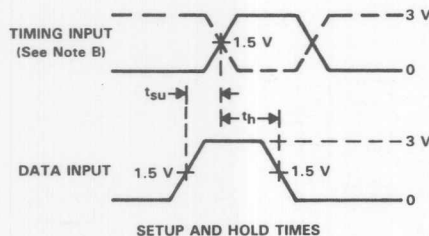
C. The outputs are measured one at a time with one input transition per measurement.

SERIES 54ACT11XXX AND 74ACT11XXX DEVICES



LOAD CIRCUIT FOR THREE-STATE OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND

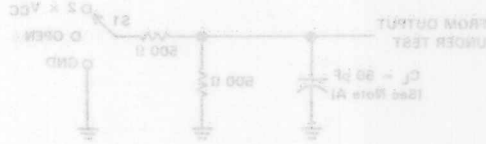


- NOTES: A. C_L includes probe and jig capacitance.
- B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$. For testing pulse duration: $t_r = 1 \text{ to } 3 \text{ ns}$, $t_f = 1 \text{ to } 3 \text{ ns}$. Pulse polarity may be either a high-to-low-to-high or low-to-high-to-low.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one input transition per measurement.

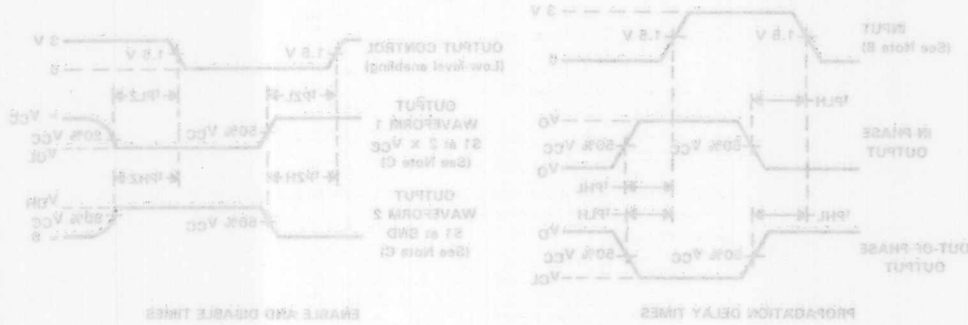
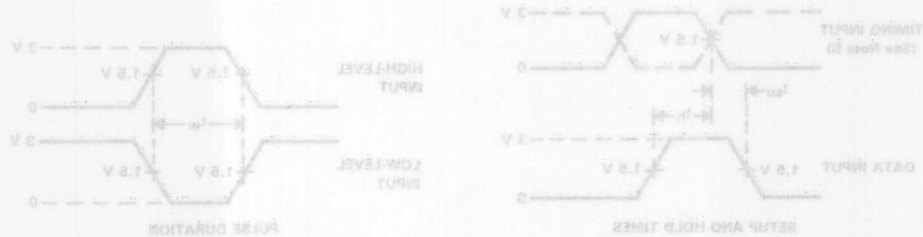
SERIES BA6211XX AND JA6211XX DEVICES

General Information

TEST	TEST
PLH-PHASE	PLH-PHASE
PLH-DUTY	PLH-DUTY
PLH-FREQ	PLH-FREQ
PLH-SETUP	PLH-SETUP
PLH-HOLD	PLH-HOLD
PLH-PROP	PLH-PROP
PLH-ENR	PLH-ENR
PLH-ENR2	PLH-ENR2
PLH-ENR3	PLH-ENR3
PLH-ENR4	PLH-ENR4
PLH-ENR5	PLH-ENR5
PLH-ENR6	PLH-ENR6
PLH-ENR7	PLH-ENR7
PLH-ENR8	PLH-ENR8
PLH-ENR9	PLH-ENR9
PLH-ENR10	PLH-ENR10
PLH-ENR11	PLH-ENR11
PLH-ENR12	PLH-ENR12
PLH-ENR13	PLH-ENR13
PLH-ENR14	PLH-ENR14
PLH-ENR15	PLH-ENR15
PLH-ENR16	PLH-ENR16
PLH-ENR17	PLH-ENR17
PLH-ENR18	PLH-ENR18
PLH-ENR19	PLH-ENR19
PLH-ENR20	PLH-ENR20
PLH-ENR21	PLH-ENR21
PLH-ENR22	PLH-ENR22
PLH-ENR23	PLH-ENR23
PLH-ENR24	PLH-ENR24
PLH-ENR25	PLH-ENR25
PLH-ENR26	PLH-ENR26
PLH-ENR27	PLH-ENR27
PLH-ENR28	PLH-ENR28
PLH-ENR29	PLH-ENR29
PLH-ENR30	PLH-ENR30
PLH-ENR31	PLH-ENR31
PLH-ENR32	PLH-ENR32
PLH-ENR33	PLH-ENR33
PLH-ENR34	PLH-ENR34
PLH-ENR35	PLH-ENR35
PLH-ENR36	PLH-ENR36
PLH-ENR37	PLH-ENR37
PLH-ENR38	PLH-ENR38
PLH-ENR39	PLH-ENR39
PLH-ENR40	PLH-ENR40
PLH-ENR41	PLH-ENR41
PLH-ENR42	PLH-ENR42
PLH-ENR43	PLH-ENR43
PLH-ENR44	PLH-ENR44
PLH-ENR45	PLH-ENR45
PLH-ENR46	PLH-ENR46
PLH-ENR47	PLH-ENR47
PLH-ENR48	PLH-ENR48
PLH-ENR49	PLH-ENR49
PLH-ENR50	PLH-ENR50
PLH-ENR51	PLH-ENR51
PLH-ENR52	PLH-ENR52
PLH-ENR53	PLH-ENR53
PLH-ENR54	PLH-ENR54
PLH-ENR55	PLH-ENR55
PLH-ENR56	PLH-ENR56
PLH-ENR57	PLH-ENR57
PLH-ENR58	PLH-ENR58
PLH-ENR59	PLH-ENR59
PLH-ENR60	PLH-ENR60
PLH-ENR61	PLH-ENR61
PLH-ENR62	PLH-ENR62
PLH-ENR63	PLH-ENR63
PLH-ENR64	PLH-ENR64
PLH-ENR65	PLH-ENR65
PLH-ENR66	PLH-ENR66
PLH-ENR67	PLH-ENR67
PLH-ENR68	PLH-ENR68
PLH-ENR69	PLH-ENR69
PLH-ENR70	PLH-ENR70
PLH-ENR71	PLH-ENR71
PLH-ENR72	PLH-ENR72
PLH-ENR73	PLH-ENR73
PLH-ENR74	PLH-ENR74
PLH-ENR75	PLH-ENR75
PLH-ENR76	PLH-ENR76
PLH-ENR77	PLH-ENR77
PLH-ENR78	PLH-ENR78
PLH-ENR79	PLH-ENR79
PLH-ENR80	PLH-ENR80
PLH-ENR81	PLH-ENR81
PLH-ENR82	PLH-ENR82
PLH-ENR83	PLH-ENR83
PLH-ENR84	PLH-ENR84
PLH-ENR85	PLH-ENR85
PLH-ENR86	PLH-ENR86
PLH-ENR87	PLH-ENR87
PLH-ENR88	PLH-ENR88
PLH-ENR89	PLH-ENR89
PLH-ENR90	PLH-ENR90
PLH-ENR91	PLH-ENR91
PLH-ENR92	PLH-ENR92
PLH-ENR93	PLH-ENR93
PLH-ENR94	PLH-ENR94
PLH-ENR95	PLH-ENR95
PLH-ENR96	PLH-ENR96
PLH-ENR97	PLH-ENR97
PLH-ENR98	PLH-ENR98
PLH-ENR99	PLH-ENR99
PLH-ENR100	PLH-ENR100



LOAD CIRCUIT FOR THREE-STATE OUTPUTS



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $V_L = 50$ V, $V_H = 3$ V. For test pulse duration: $t_p = 1$ to 3 ns. Pulse duty cycle may be either a high-to-low or low-to-high-to-low.
 - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. The outputs are measured one at a time with one input transition per measurement.

GATES AND INVERTERS WITH TWO-STATE OUTPUTS

POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	AVAILABILITY
Hex inverter	004	▲
Hex noninverter	034	▲
Triple 3-input gate	010	●
Dual 4-input gate	020	●
8-input gate	030	●

POSITIVE-AND GATES

DESCRIPTION	TYPE	AVAILABILITY
Quadruple 2-input gate	008	●
Triple 3-input gate	011	●
Dual 4-input gate	021	●

POSITIVE-NOR GATES

DESCRIPTION	TYPE	AVAILABILITY
Quadruple 2-input gate	002	●
Triple 3-input gate	027	●

POSITIVE-OR GATES

DESCRIPTION	TYPE	AVAILABILITY
Quadruple 2-input gate	032	●

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	AVAILABILITY
Hex inverter	014	▲
Dual 4-input positive NAND	013	▲
Quadruple 2-input positive NAND	132	▲

● Denotes available product.

▲ Denotes planned new products. For product availability on these devices, contact the factory.

BUFFERS, DRIVERS, AND TRANSCEIVERS WITH THREE-STATE OUTPUTS

BUFFERS, DRIVERS, AND TRANSCEIVERS

DESCRIPTION	# of BITS	TYPE	AVAILABILITY	
			AC	ACT
Noninverting buffer/driver	10	827	▲	▲
	8	241	●	●
	8	244	●	●
Inverting buffer/driver	10	828	▲	▲
	8	240	●	●
Noninverting transceiver	10	861	▲	▲
	9	863	▲	▲
Inverting transceiver	10	862	▲	▲
	9	864	▲	▲

8-BIT BIDIRECTIONAL BUS TRANSCEIVERS

DESCRIPTION	TYPE	AVAILABILITY	
		AC	ACT
Noninverting	245	▲	●
	623	▲	▲
	652	▲	▲
Inverting	620	▲	▲
	651	▲	▲
	640	▲	▲
Inverting and noninverting	643	▲	▲
Noninverting registered	646	▲	▲
Inverting registered	648	▲	▲
Noninverting with parity	657	▲	▲
Noninverting registered	833	▲	▲
Inverting registered	834	▲	▲
Noninverting latched	853	▲	▲
Inverting latched	854	▲	▲

● Denotes available product.

▲ Denotes planned new products. For product availability on these devices, contact the factory.

COUNTERS FLIP-FLOPS

DUAL AND SINGLE FLIP-FLOPS WITH ASYNC CLEAR AND PRESET

DESCRIPTION	TYPE	CLOCK EDGE	AVAILABILITY	
			AC	ACT
Dual J-K edge triggered	109	POS	●	●
Dual D-type	112	NEG	▲	▲
	074	POS	●	●

QUAD AND HEX FLIP-FLOPS WITH POSITIVE CLOCK EDGE

DESCRIPTION	OUTPUT	# of F:F	CLEAR	TYPE	AVAILABILITY	
					AC	ACT
D-type	Q	6	ASYNC	174	▲	▲
	Q	6	—	378	▲	▲
	Q, \bar{Q}	4	ASYNC	175	▲	▲
	Q, \bar{Q}	4	—	379	▲	▲

8-, 9-, and 10-BIT D-TYPE FLIP-FLOPS WITH THREE-STATE OUTPUTS

DESCRIPTION	# OF BITS	CLEAR	CLOCK EDGE	TYPE	AVAILABILITY	
					AC	ACT
Noninverting	8	—	POS	374	▲	●
Noninverting dual 4-bit	8	ASYNC	POS	874	▲	▲
Inverting	8	—	POS	534	▲	▲
Noninverting	8	ASYNC	POS	825	▲	▲
Inverting	8	ASYNC	POS	826	▲	▲
Noninverting	9	ASYNC	POS	823	▲	▲
Inverting	9	ASYNC	POS	824	▲	▲
Noninverting	10	—	POS	821	▲	▲
Inverting	10	—	POS	822	▲	▲

● Denotes available product.

▲ Denotes planned new products. For product availability on these devices, contact the factory.

COUNTERS AND LATCHES

SYNCHRONOUS COUNTERS WITH POSITIVE-EDGE CLOCK

DESCRIPTION	# OF BITS	OUTPUT	CLEAR	PARALLEL LOAD	TYPE	AVAILABILITY	
						AC	ACT
Decade	4	TOTEM-POLE	ASYN	SYNC	160	▲	▲
	4	TOTEM-POLE	SYNC	SYNC	162	▲	▲
Decade up/down	4	TOTEM-POLE	—	SYNC	168	▲	▲
	4	TOTEM-POLE	—	ASYN	190	▲	▲
	4	TOTEM-POLE	ASYN	ASYN	192	▲	▲
	4	TOTEM-POLE	BOTH	SYNC	568	▲	▲
Binary	4	TOTEM-POLE	ASYN	SYNC	161	▲	▲
	4	TOTEM-POLE	SYNC	SYNC	163	▲	▲
Binary up/down	4	TOTEM-POLE	—	SYNC	169	▲	▲
	4	TOTEM-POLE	—	ASYN	191	▲	▲
	4	TOTEM-POLE	ASYN	ASYN	193	▲	▲
	4	3-STATE	BOTH	SYNC	569	▲	▲
Bidirectional binary	8	TOTEM-POLE	—	SYNC	269	▲	▲
	8	3-STATE	BOTH	SYNC (I/O)	579	▲	▲

8-, 9-, AND 10-BIT LATCHES WITH THREE-STATE OUTPUTS

DESCRIPTION	# OF BITS	CLEAR	PRESET	TYPE	AVAILABILITY	
					AC	ACT
Transparent	8	—	—	373	●	●
Noninverting dual 4-bit	8	X	—	873	▲	▲
Inverting	8	—	—	533	●	●
Noninverting	8	X	X	845	▲	▲
Inverting	8	X	X	846	▲	▲
Noninverting	9	X	X	843	▲	▲
Inverting	9	X	X	844	▲	▲
Noninverting	10	—	—	841	▲	▲
Inverting	10	—	—	842	▲	▲

● Denotes available product.

▲ Denotes planned new products. For product availability on these devices, contact the factory.

DATA SELECTORS/MULTIPLEXERS AND DECODERS/DEMULTIPLEXERS

DATA SELECTORS/MULTIPLEXERS

DESCRIPTION	OUTPUT	TYPE	AVAILABILITY	
			AC	ACT
8-to-1	TOTEM-POLE	151	▲	▲
	3-STATE	251	▲	▲
Dual 4-to-1	TOTEM-POLE	153	▲	▲
	3-STATE	253	▲	▲
	TOTEM-POLE	352	▲	▲
	TOTEM-POLE	353	▲	▲
	TOTEM-POLE	157	▲	▲
Quad 2-to-1	TOTEM-POLE	158	▲	▲
	3-STATE	257	▲	▲
	3-STATE	258	▲	▲

DECODERS/DEMULTIPLEXERS WITH TWO-STATE OUTPUTS

DESCRIPTION	TYPE	AVAILABILITY	
		AC	ACT
3-to-8	138	▲	▲
Dual 2-to-4	139	▲	▲
3-to-8	238	▲	▲
Dual 2-to-4	239	▲	▲

● Denotes available product.

▲ Denotes planned new products. For product availability on these devices, contact the factory.

REGISTERS WITH POSITIVE-CLOCK EDGE

SHIFT REGISTERS

DESCRIPTION	OUTPUT	# OF BITS	MODES					TYPE	AVAILABILITY	
			SR	SL	LOAD	HOLD	CLEAR		AC	ACT
Parallel in	3-STATE	8	X	X	X	X	ASYNC	299	▲	▲
Parallel out	3-STATE	8	X	X	X	X	SYNC	323	▲	▲
Bidirectional	TOTEM-POLE	4	X	X	X	X	ASYNC	194	▲	▲

OTHER REGISTERS

DESCRIPTION	OUTPUT	# OF BITS	MODES					TYPE	AVAILABILITY	
			SR	SL	LOAD	HOLD	CLEAR		AC	ACT
Universal	3-STATE	8	X	X	X	X	ASYNC	299	▲	▲
	3-STATE	8	X	X	X	X	SYNC	323	▲	▲
Diagnostic/pipeline	3-STATE	8	X	—	—	—	—	818	▲	▲
818 w/parity	3-STATE	8	X	—	—	—	—	819	▲	▲

DESCRIPTION	TYPE	AVAILABILITY
3-to-8	851	▲
8-to-3	851	▲
3-to-8	851	▲
8-to-3	851	▲

● Denotes available product.

▲ Denotes planned new products. For product availability on these devices, contact the factory.

ARITHMETIC LOGIC UNITS, COMPARATORS, AND PARITY GENERATORS/CHECKERS

ARITHMETIC LOGIC UNITS AND LOOK-AHEAD CARRY GENERATORS

DESCRIPTION	OUTPUT	TYPE	AVAILABILITY	
			AC	ACT
4-bit ALU/function generator	TOTEM-POLE	181	▲	▲
	TOTEM-POLE	881	▲	▲
32-bit look-ahead carry generator	TOTEM-POLE	882	▲	▲

COMPARATORS WITH TWO-STATE OUTPUTS

DESCRIPTION	# BITS	$\bar{P}=\bar{Q}$	$P=Q$	$\bar{P}>\bar{Q}$	$P>Q$	$P<Q$	TYPE	AVAILABILITY	
								AC	ACT
20-k Ω pull-up	8	NO	YES	NO	NO	NO	520	●	●
Standard	8	NO	YES	NO	NO	NO	521	●	●

9-BIT PARITY GENERATORS/CHECKERS
WITH TWO-STATE OUTPUTS

DESCRIPTION	TYPE	AVAILABILITY	
		AC	ACT
Odd/Even parity	280	▲	▲
Generators/Checkers	286	▲	▲

● Denotes available product.

▲ Denotes planned new products. For product availability on these devices, contact the factory.

ARITHMETIC LOGIC UNITS, COMPARATORS, AND PARITY GENERATORS/CHECKERS

ARITHMETIC LOGIC UNITS AND LOOK-AHEAD CARRY GENERATORS

DESCRIPTION	OUTPUT	TYPE	AVAILABILITY
4-bit ALU/Function Generator	TOTEM-POLE	181	Δ
4-bit ALU/Function Generator	TOTEM-POLE	281	Δ
32-bit look-ahead carry generator	TOTEM-POLE	885	Δ

COMPARATORS WITH TWO-STATE OUTPUTS

DESCRIPTION	W	P=Q	P<Q	P>Q	R<Q	TYPE	AVAILABILITY
20-kb pull-up	5	NO	YES	NO	NO	520	●
Random	8	NO	YES	NO	NO	521	●

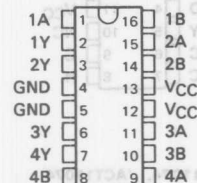
2-BIT PARITY GENERATORS/CHECKERS WITH TWO-STATE OUTPUTS

DESCRIPTION	TYPE	AVAILABILITY
Odd/Even parity Generator/Checker	280	Δ
Generator/Checker	288	Δ

© Denotes obsolete product.
Δ Denotes planned new product. For product availability on these devices, contact the factory.

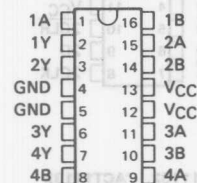
'AC11000, 'ACT11000
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

(TOP VIEW)



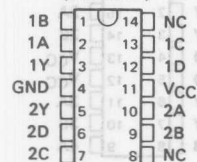
'AC11008, 'ACT11008
QUADRUPLE 2-INPUT
POSITIVE-AND GATES

(TOP VIEW)



'AC11013, 'ACT11013
DUAL 4-INPUT GATES

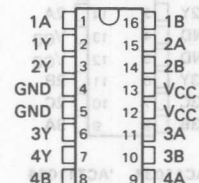
(TOP VIEW)



EPIC™ACL PINOUTS

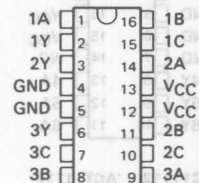
'AC11002, 'ACT11002
QUADRUPLE 2-INPUT
POSITIVE-NOR GATES

(TOP VIEW)



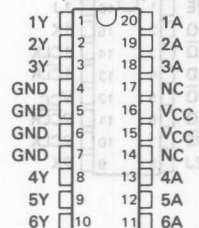
'AC11010, 'ACT11010
TRIPLE 3-INPUT
POSITIVE-NAND GATES

(TOP VIEW)



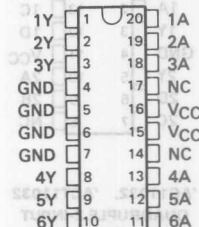
'AC11014, 'ACT11014
HEX INVERTERS

(TOP VIEW)



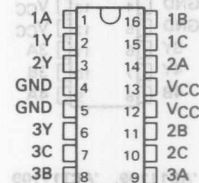
'AC11004, 'ACT11004
HEX INVERTERS

(TOP VIEW)



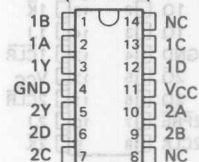
'AC11011, 'ACT11011
TRIPLE 3-INPUT
POSITIVE-AND GATES

(TOP VIEW)

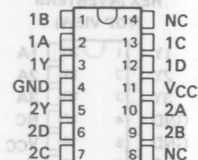


'AC11020, 'ACT11020
DUAL 4-INPUT
POSITIVE-NAND GATES

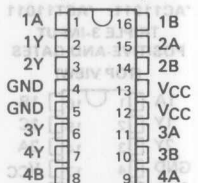
(TOP VIEW)



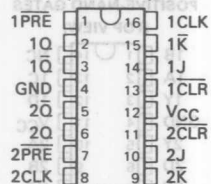
'AC11021, 'ACT11021
DUAL 4-INPUT
POSITIVE-AND GATES
(TOP VIEW)



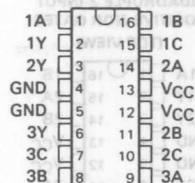
'AC11032, 'ACT11032
QUADRUPLE 2-INPUT
POSITIVE-OR GATES
(TOP VIEW)



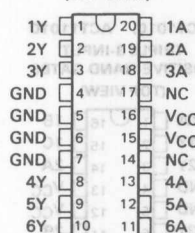
'AC11109, 'ACT11109
DUAL J-K
POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH CLEAR AND PRESET
(TOP VIEW)



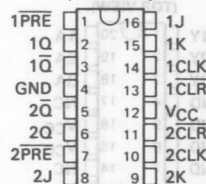
'AC11027, 'ACT11027
TRIPLE 3-INPUT
POSITIVE-NOR GATES
(TOP VIEW)



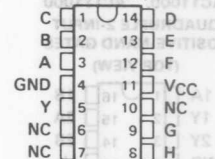
'AC11034, 'ACT11034
HEX NONINVERTERS
(TOP VIEW)



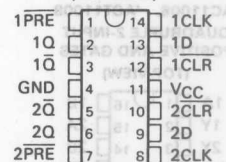
'AC11112, 'ACT11112
DUAL J-K NEGATIVE
EDGE-TRIGGERED FLIP-FLOPS
WITH CLEAR AND PRESET
(TOP VIEW)



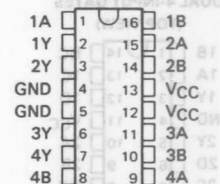
'AC11030, 'ACT11030
8-INPUT POSITIVE-NAND GATES
(TOP VIEW)



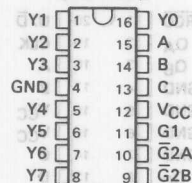
'AC11074, 'ACT11074
DUAL D-TYPE POSITIVE-EDGE TRIGGERED
FLIP-FLOPS WITH CLEAR AND PRESET
(TOP VIEW)



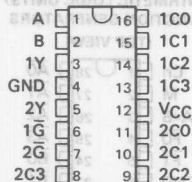
'AC11132, 'ACT11132
QUADRUPLE 2-INPUT
POSITIVE-NAND SCHMITT TRIGGERS
(TOP VIEW)



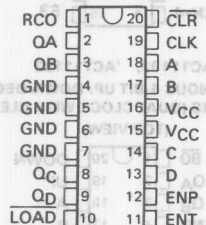
'AC11138, 'ACT11138
3-LINE TO 8-LINE
DECODERS/DEMULTIPLEXERS
(TOP VIEW)



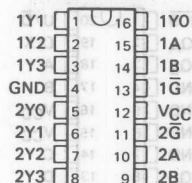
'AC11153, 'ACT11153
DUAL 4-LINE TO 1-LINE DATA
SELECTORS/MULTIPLEXERS
(TOP VIEW)



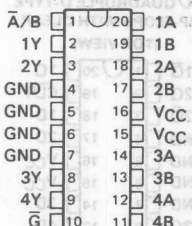
'AC11160, 'ACT11160
SYNCHRONOUS 4-BIT
BINARY COUNTERS
(TOP VIEW)



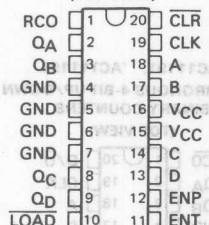
'AC11139, 'ACT11139
DUAL 2-LINE TO 4-LINE
DECODERS/DEMULTIPLEXERS
(TOP VIEW)



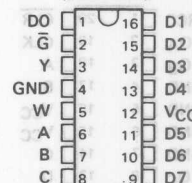
'AC11157, 'ACT11157
QUADRUPLE 1 OF 2
DATA SELECTORS/MULTIPLEXERS
(TOP VIEW)



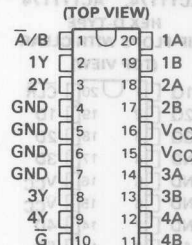
'AC11161, 'ACT11161
SYNCHRONOUS 4-BIT
DECADE COUNTERS
(TOP VIEW)



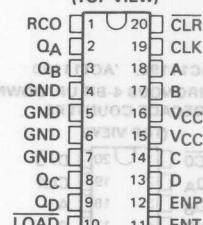
'AC11151, 'ACT11151
1 OF 8 DATA
SELECTORS/MULTIPLEXERS
(TOP VIEW)



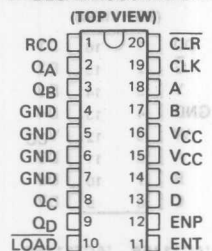
'AC11158, 'ACT11158
QUADRUPLE 1 OF 2 DATA
SELECTORS/MULTIPLEXERS
(TOP VIEW)



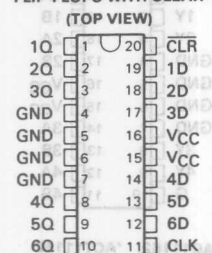
'AC11162, 'ACT11162
SYNCHRONOUS 4-BIT
BINARY COUNTERS
(TOP VIEW)



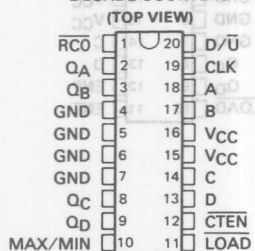
'AC11163, 'ACT11163
SYNCHRONOUS 4-BIT
DECADE COUNTERS



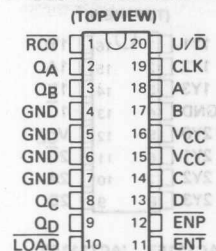
'AC11174, 'ACT11174
HEX D-TYPE
FLIP-FLOPS WITH CLEAR



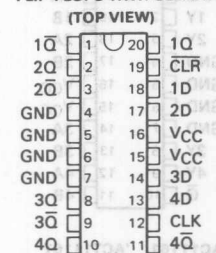
'AC11190, 'ACT11190
SYNCHRONOUS 4-BIT UP/DOWN
DECADE COUNTERS



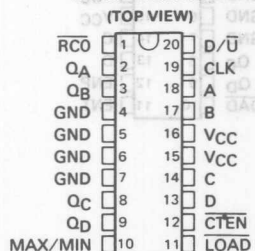
'AC11168, 'ACT11168
SYNCHRONOUS 4-BIT UP/DOWN
DECADE COUNTERS



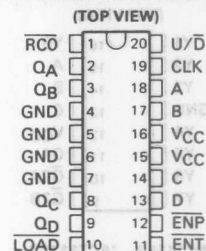
'AC11175, 'ACT11175
HEX/QUADRUPLE D-TYPE
FLIP-FLOPS WITH CLEAR



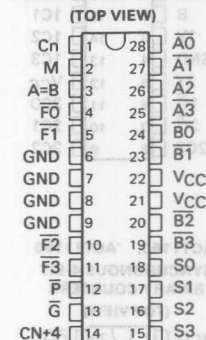
'AC11191, 'ACT11191
SYNCHRONOUS 4-BIT UP/DOWN
BINARY COUNTERS



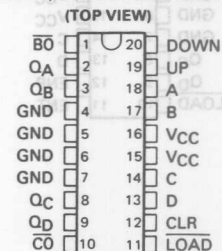
'AC11169, 'ACT11169
SYNCHRONOUS 4-BIT UP/DOWN
BINARY COUNTERS



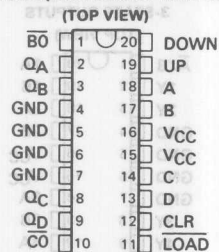
'AC11181, 'ACT11181
ARITHMETIC LOGIC UNITS/
FUNCTION GENERATORS



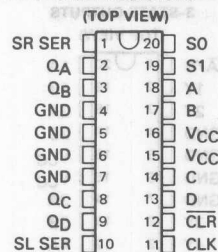
'AC11192, 'ACT11192
SYNCHRONOUS 4-BIT UP/DOWN DECADE
COUNTERS (DUAL CLOCK WITH CLEAR)



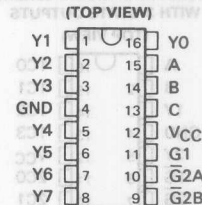
'AC11193, 'ACT11193
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS (DUAL CLOCK WITH CLEAR)



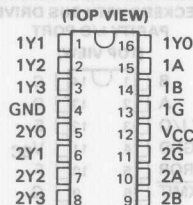
'AC11194, 'ACT11194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS



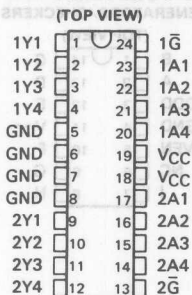
'AC11238, 'ACT11238
3-LINE TO 8-LINE DECODERS/DEMULPLEXERS



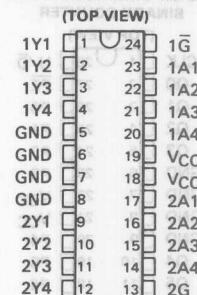
'AC11239, 'ACT11239
DUAL 2-LINE TO 4-LINE DECODERS/DEMULPLEXERS



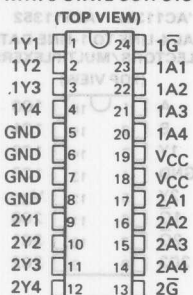
'AC11240, 'ACT11240
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS



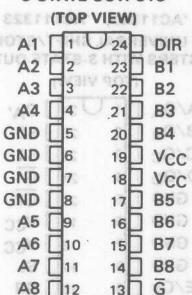
'AC11241, 'ACT11241
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS



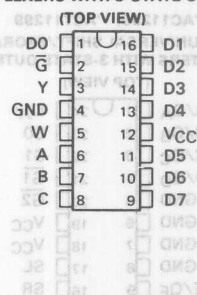
'AC11244, 'ACT11244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS



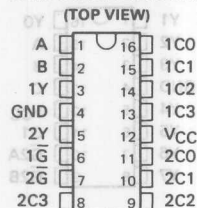
'AC11245, 'ACT11245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



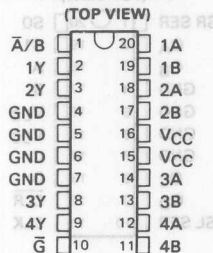
'AC11251, 'ACT11251
1 OF 8 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS



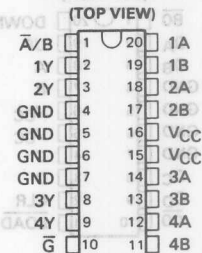
'AC11253, 'ACT11253
DUAL 4-LINE TO 1-LINE DATA
SELECTORS/MULTIPLEXERS
WITH 3-STATE OUTPUTS



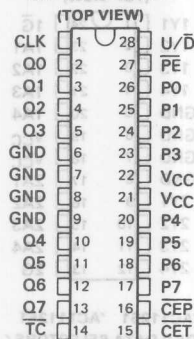
'AC11257, 'ACT11257
QUADRUPLE 1 OF 2 DATA
SELECTORS/MULTIPLEXERS WITH
3-STATE OUTPUTS



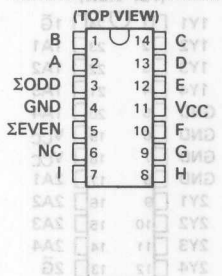
'AC11258, 'ACT11258
QUADRUPLE 1 OF 2 DATA
SELECTORS/MULTIPLEXERS WITH
3-STATE OUTPUTS



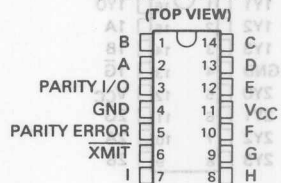
'AC11269, 'ACT11269
8-BIT BIDIRECTIONAL
BINARY COUNTER



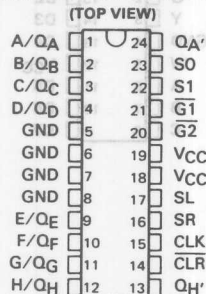
'AC11280, 'ACT11280
9-BIT PARITY
GENERATORS/CHECKERS



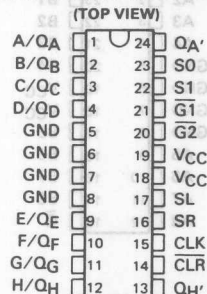
'AC11286, 'ACT11286
9-BIT PARITY GENERATORS/
CHECKERS WITH BUS DRIVER
PARITY I/O PORT



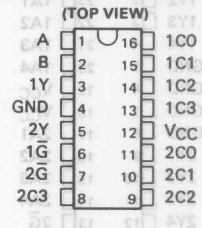
'AC11299, 'ACT11299
8-BIT UNIVERSAL SHIFT/STORAGE
REGISTERS WITH 3-STATE OUTPUTS



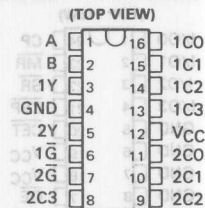
'AC11323, 'ACT11323
8-BIT UNIVERSAL SHIFT/STORAGE
REGISTERS WITH 3-STATE OUTPUTS



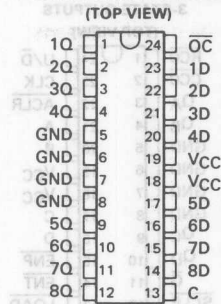
'AC11352, 'ACT11352
DUAL 4-LINE TO 1-LINE DATA
SELECTORS/MULTIPLEXERS



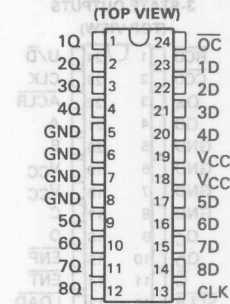
'AC11353, 'ACT11353
DUAL 1 OF 4 DATA SELECTORS/
MULTIPLEXERS WITH 3-STATE OUTPUTS



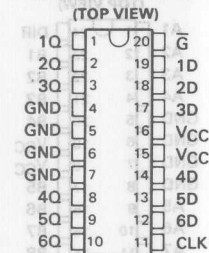
'AC11373, 'ACT11373
OCTAL D-TYPE TRANSPARENT LATCHES
WITH 3-STATE OUTPUTS



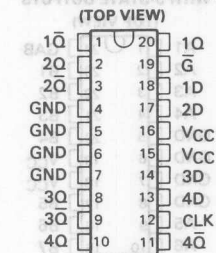
'AC11374, 'ACT11374
OCTAL D-TYPE EDGE-TRIGGERED
FLIP-FLOPS



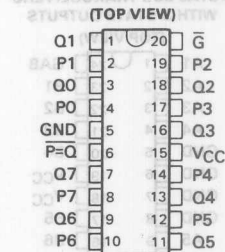
'AC11378, 'ACT11378
HEX D-TYPE FLIP-FLOPS
WITH CLOCK ENABLE



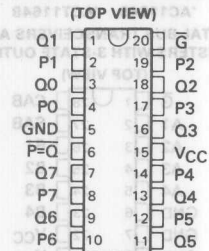
'AC11379, 'ACT11379
QUADRUPLE D-TYPE
FLIP-FLOPS WITH CLEAR



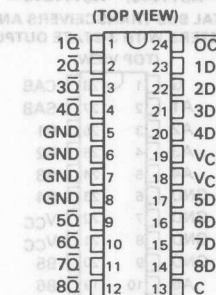
'AC11520, 'ACT11520
8-BIT IDENTITY COMPARATOR



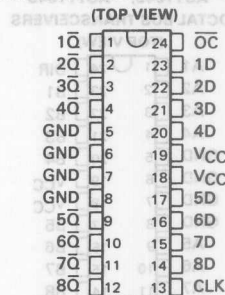
'AC11521, 'ACT11521
8-BIT IDENTITY COMPARATOR



'AC11533, 'ACT11533
OCTAL D-TYPE TRANSPARENT
LATCHES WITH 3-STATE OUTPUT



'AC11534, 'ACT11534
OCTAL D-TYPE EDGE-TRIGGERED
FLIP-FLOPS WITH 3-STATE OUTPUT

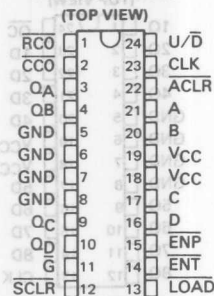


DEVICE PIN-OUTS

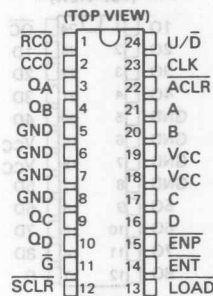
1

General Information

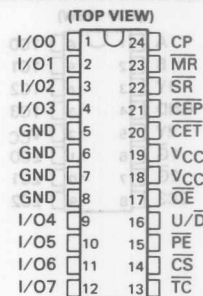
'AC11568, 'ACT11568
SYNCHRONOUS 4-BIT UP/DOWN
DECADE COUNTERS WITH
3-STATE OUTPUTS



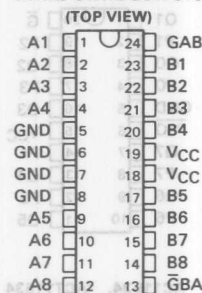
'AC11569, 'ACT11569
SYNCHRONOUS 4-BIT UP/DOWN
BINARY COUNTERS WITH
3-STATE OUTPUTS



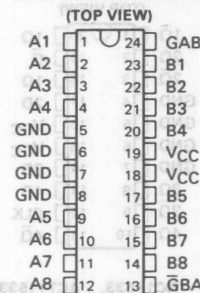
'AC11579, 'ACT11579
8-BIT BIDIRECTIONAL BINARY
COUNTER WITH 3-STATE OUTPUTS



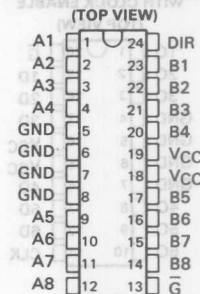
'AC11620, 'ACT11620
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS



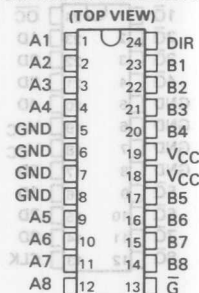
'AC11623, 'ACT11623
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS



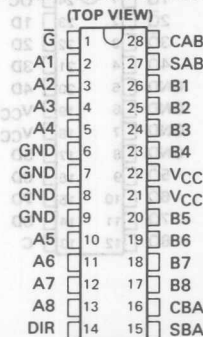
'AC11640, 'ACT11640
OCTAL BUS TRANSCEIVERS



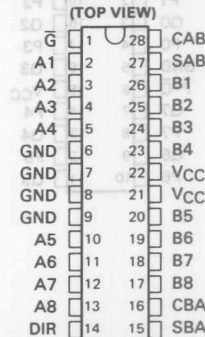
'AC11643, 'ACT11643
OCTAL BUS TRANSCEIVERS



'AC11646, 'ACT11646
OCTAL BUS TRANSCEIVERS AND
REGISTERS WITH 3-STATE OUTPUTS



'AC11648, 'ACT11648
OCTAL BUS TRANSCEIVERS AND
REGISTERS WITH 3-STATE OUTPUTS



'AC11651, 'ACT11651

OCTAL BUS TRANSCEIVERS
AND REGISTERS

(TOP VIEW)

GAB	1	28	CAB
A1	2	27	SAB
A2	3	26	B1
A3	4	25	B2
A4	5	24	B3
GND	6	23	B4
GND	7	22	VCC
GND	8	21	VCC
GND	9	20	B5
A5	10	19	B6
A6	11	18	B7
A7	12	17	B8
A8	13	16	CBA
GBA	14	15	SBA

'AC11652, 'ACT11652

OCTAL BUS TRANSCEIVERS
AND REGISTERS

(TOP VIEW)

GAB	1	28	CAB
A1	2	27	SAB
A2	3	26	B1
A3	4	25	B2
A4	5	24	B3
GND	6	23	B4
GND	7	22	VCC
GND	8	21	VCC
GND	9	20	B5
A5	10	19	B6
A6	11	18	B7
A7	12	17	B8
A8	13	16	CBA
GBA	14	15	SBA

'AC11657, 'ACT11657

OCTAL BIDIRECTIONAL TRANSCEIVERS
WITH 8-BIT PARITY GENERATOR/CHECKER
AND 3-STATE OUTPUTS

(TOP VIEW)

PARITY/B8	1	28	OE
A0	2	27	NC
A1	3	26	BO
A2	4	25	B1
A3	5	24	B2
GND	6	23	B3
GND	7	22	VCC
GND	8	21	VCC
GND	9	20	B4
A4	10	19	B5
A5	11	18	B6
A6	12	17	B7
A7	13	16	EVEN/ODD
ERROR	14	15	T/R

'AC11818, 'ACT11818

DIAGNOSTIC/PIPELINE REGISTER

(TOP VIEW)

OC	1	28	DCLK
1Q	2	27	MODE
2Q	3	26	1D
3Q	4	25	2D
4Q	5	24	3D
GND	6	23	4D
GND	7	22	VCC
GND	8	21	VCC
GND	9	20	5D
5Q	10	19	6D
6Q	11	18	7D
7Q	12	17	8D
8Q	13	16	SDI
SDO	14	15	PCLK

'AC11819, 'ACT11819

DIAGNOSTIC/PIPELINE REGISTER

(TOP VIEW)

OC	1	28	DCLK
1Q	2	27	MODE
2Q	3	26	1D
3Q	4	25	2D
4Q	5	24	3D
GND	6	23	4D
GND	7	22	VCC
GND	8	21	VCC
GND	9	20	5D
5Q	10	19	6D
6Q	11	18	7D
7Q	12	17	8D
8Q	13	16	SDI
SDO	14	15	PCLK

'AC11821, 'ACT11821

10-BIT BUS INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS

(TOP VIEW)

1Q	1	28	OC
2Q	2	27	1D
3Q	3	26	2D
4Q	4	25	3D
5Q	5	24	4D
GND	6	23	5D
GND	7	22	VCC
GND	8	21	VCC
GND	9	20	6D
6Q	10	19	7D
7Q	11	18	8D
8Q	12	17	9D
9Q	13	16	10D
10Q	14	15	CLK

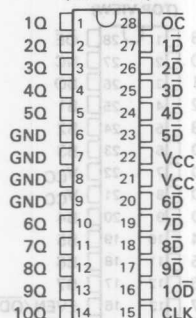
DEVICE PIN-OUTS

1

General Information

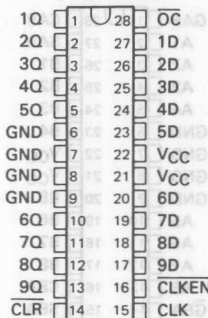
'AC11822, 'ACT11822
10-BIT BUS INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS

(TOP VIEW)



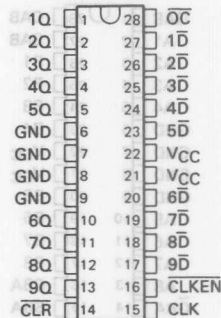
'AC11823, 'ACT11823
9-BIT BUS INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS

(TOP VIEW)



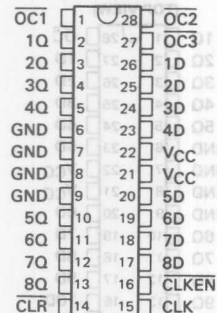
'AC11824, 'ACT11824
9-BIT BUS INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS

(TOP VIEW)



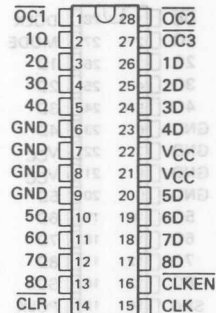
'AC11825, 'ACT11825
8-BIT BUS INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS

(TOP VIEW)



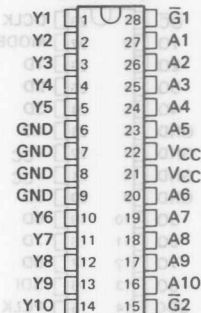
'AC11826, 'ACT11826
8-BIT BUS INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS

(TOP VIEW)

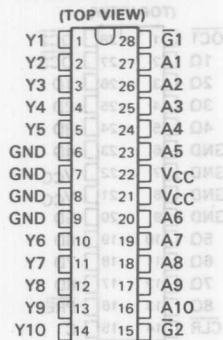


'AC11827, 'ACT11827
10-BIT BUFFERS WITH
3-STATE OUTPUTS

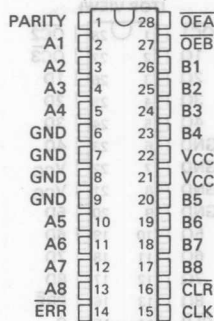
(TOP VIEW)



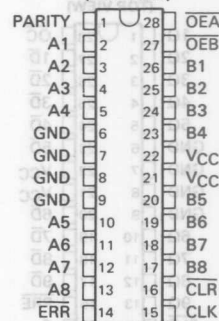
'AC11828, 'ACT11828
10-BIT BUFFERS WITH
3-STATE OUTPUTS



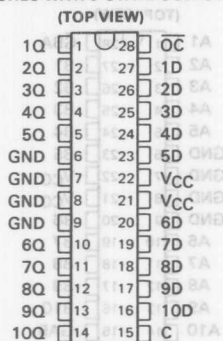
'AC11833, 'ACT11833
PARITY BUS TRANSCEIVERS
(TOP VIEW)



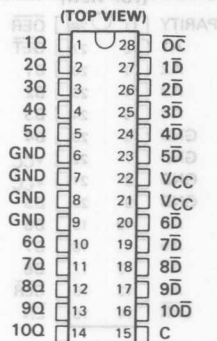
'AC11834, 'ACT11834
PARITY BUS TRANSCEIVERS
(TOP VIEW)



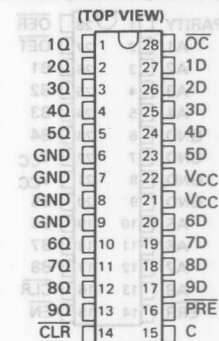
'AC11841, 'ACT11841
10-BIT BUS INTERFACE D-TYPE
LATCHES WITH 3-STATE OUTPUTS



'AC11842, 'ACT11842
10-BIT BUS INTERFACE D-TYPE
LATCHES WITH 3-STATE OUTPUTS



'AC11843, 'ACT11843
9-BIT BUS INTERFACE D-TYPE
LATCHES WITH 3-STATE OUTPUTS



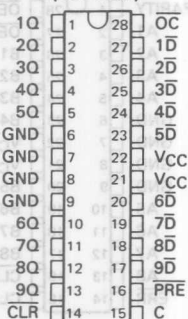
DEVICE PIN-OUTS

1

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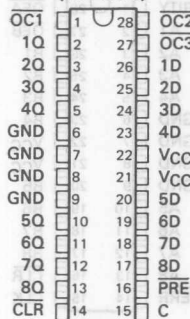
'AC11844, 'ACT11844
9-BIT BUS INTERFACE D-TYPE
LATCHES WITH 3-STATE OUTPUTS

(TOP VIEW)



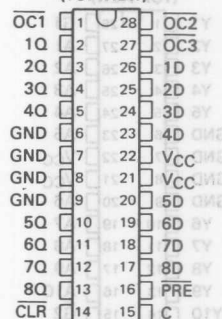
'AC11845, 'ACT11845
8-BIT BUS INTERFACE D-TYPE
LATCHES WITH 3-STATE OUTPUTS

(TOP VIEW)

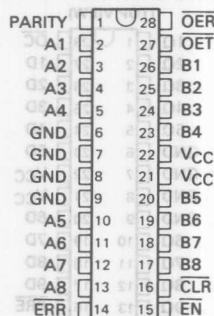


'AC11846, 'ACT11846
8-BIT BUS INTERFACE D-TYPE
LATCHES WITH 3-STATE OUTPUTS

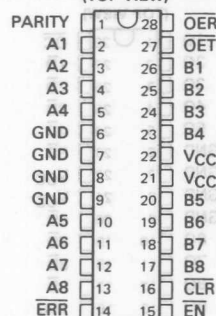
(TOP VIEW)



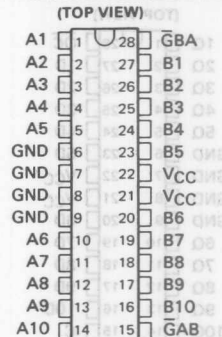
'AC11853, 'ACT11853
PARITY BUS TRANSCEIVERS
(TOP VIEW)



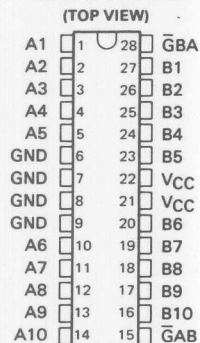
'AC11854, 'ACT11854
PARITY BUS TRANSCEIVERS
(TOP VIEW)



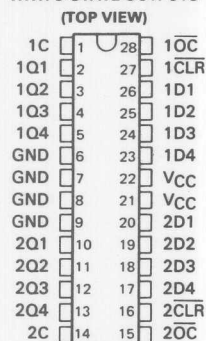
'AC11861, 'ACT11861
10-BIT BUS TRANSCEIVERS WITH
3-STATE OUTPUTS
(TOP VIEW)



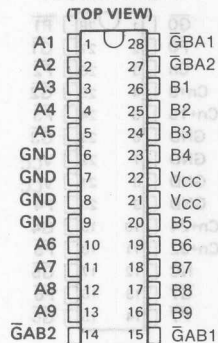
'AC11862, 'ACT11862
10-BIT BUS TRANSCEIVERS WITH
3-STATE OUTPUTS



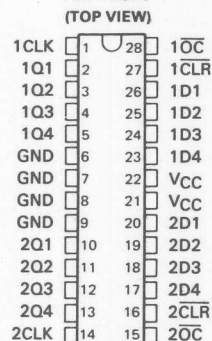
'AC11873, 'ACT11873
DUAL 4-BIT D-TYPE LATCHES
WITH 3-STATE OUTPUTS



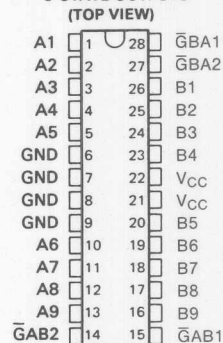
'AC11863, 'ACT11863
9-BIT BUS TRANSCEIVERS WITH
3-STATE OUTPUTS



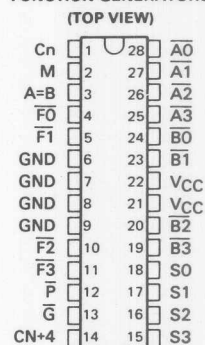
'AC11874, 'ACT11874
DUAL 4-BIT D-TYPE EDGE-TRIGGERED
FLIP-FLOPS



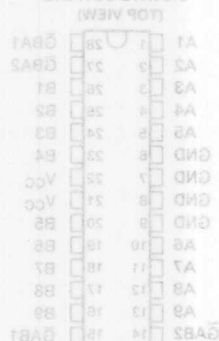
'AC11864, 'ACT11864
9-BIT BUS TRANSCEIVERS WITH
3-STATE OUTPUTS



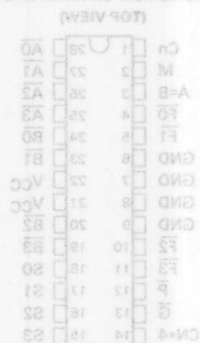
'AC11881, 'ACT11881
ARITHMETIC LOGIC UNITS/
FUNCTION GENERATORS



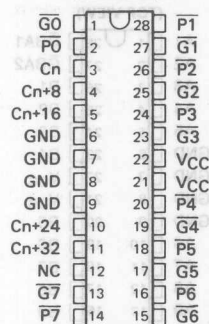
'ACT11884', 'ACT11884'
8-BIT BUS TRANSCEIVERS WITH
3-STATE OUTPUTS



'ACT11887', 'ACT11887'
ARITHMETIC LOGIC UNIT
FUNCTION GENERATORS



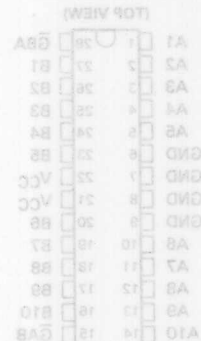
'ACT11882', 'ACT11882'
32-BIT LOOK-AHEAD CARRY GENERATORS
(TOP VIEW)



'ACT11874', 'ACT11874'
DUAL 4-BIT D-TYPE EDGE-TRIGGERED
FLIP-FLOPS



'ACT11885', 'ACT11885'
10-BIT BUS TRANSCEIVERS WITH
3-STATE OUTPUTS



'ACT11873', 'ACT11873'
DUAL 4-BIT D-TYPE LATCHES
WITH 3-STATE OUTPUTS



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Advanced CMOS Circuits

Advanced CMOS Circuits

Mechanical Data

Package Data
Ordering Instructions

54AC11000, 74AC11000 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

D2957, APRIL 1987

- New Flow-Through Architecture to Optimize PCB Layout

- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise

- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process

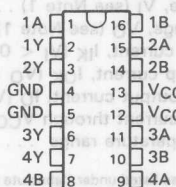
- 500-mA Typical Latch-Up Immunity at 125°C

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54AC11000 ... J PACKAGE

74AC11000 ... D OR N PACKAGE

(TOP VIEW)



54AC11000 ... FK PACKAGE

(TOP VIEW)



NC—No internal connection

description

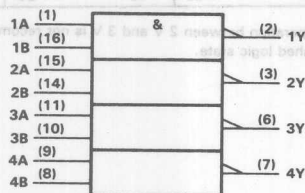
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{A + B}$ in positive logic.

The 54AC11000 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC11000 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

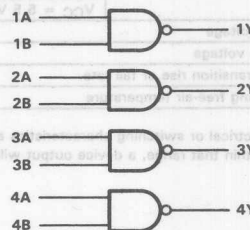
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



2

Advanced CMOS Circuits

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54AC11000, 74AC11000 QUADRUPL 2-INPUT POSITIVE-NAND GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) †

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Storage temperature range	-65°C to 150°C

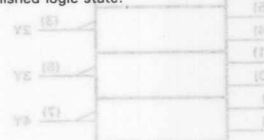
†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54AC11000			74AC11000			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 2)	3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V			2.1			V
		V _{CC} = 4.5 V			3.15			
		V _{CC} = 5.5 V			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V			0.9			V
		V _{CC} = 4.5 V			1.35			
		V _{CC} = 5.5 V			1.65			
I _{OH}	High-level output current	V _{CC} = 3 V			-4			mA
		V _{CC} = 4.5 V			-24			
		V _{CC} = 5.5 V			-24			
I _{OL}	Low-level output current	V _{CC} = 3 V			12			mA
		V _{CC} = 4.5 V			24			
		V _{CC} = 5.5 V			24			
V _I	Input voltage	0	V _{CC}		0	V _{CC}		V
V _O	Output voltage	0	V _{CC}		0	V _{CC}		V
Δt/Δv	Input transition rise or fall rate	0	10		0	10		ns/V
T _A	Operating free-air temperature	-55	125		-40	85		°C

NOTE 2: No electrical or switching characteristics are specified at $V_{CC} < 3$ V. Operation between 2 V and 3 V is not recommended, but within that range, a device output will maintain a previously established logic state.



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and H packages.

54AC11000, 74AC11000
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11000		74AC11000		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
V _{OL}	I _{OL} = 50 µA	3 V		0.1		0.1		0.1		V
		4.5 V		0.1		0.1		0.1		
		5.5 V		0.1		0.1		0.1		
	I _{OL} = 12 mA	3 V		0.36		0.5		0.44		
		4.5 V		0.36		0.5		0.44		
		5.5 V		0.36		0.5		0.44		
	I _{OL} = 50 mA†	5.5 V				1.65				
		5.5 V						1.65		
I _I	V _I = V _{CC} or GND	5.5 V		±0.1		±1		±1		µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4	80		40		µA
C _i	V _I = V _{CC} or GND	5 V		3.5						pF

†Not more than one output should be tested at one time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C			54AC11000		74AC11000		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	3.3 ± 0.3 V	1.5	7.2	9.8	1.5	11.9	1.5	11.1	ns
			5 ± 0.5 V	1.5	5	6.5	1.5	8.1	1.5	7.4	
t _{PHL}			3.3 ± 0.3 V	1.5	5.8	8.6	1.5	10.2	1.5	9.6	
			5 ± 0.5 V	1.5	4.4	6.1	1.5	7.3	1.5	6.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per gate	C _L = 50 pF, f = 1 MHz	33	pF

2

Advanced CMOS Circuits

FROM OUTPUT UNDER TEST

LOAD CIRCUIT

INPUT (See Note B)

OUTPUT

PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_0 = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

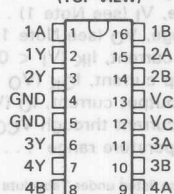
54ACT11000, 74ACT11000 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

D2957, JUNE 1987

- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

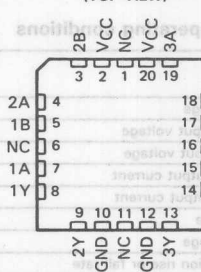
54ACT11000 ... J PACKAGE
74ACT11000 ... D OR N PACKAGE

(TOP VIEW)



54ACT11000 ... FK PACKAGE

(TOP VIEW)



NC—No internal connection

description

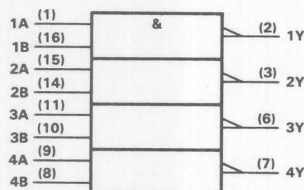
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The 54ACT11000 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74ACT11000 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

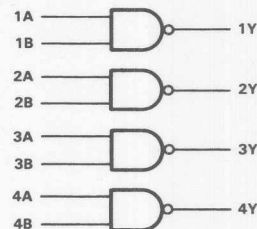
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



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54ACT11000, 74ACT11000
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	−65°C to 150°C

[†]Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

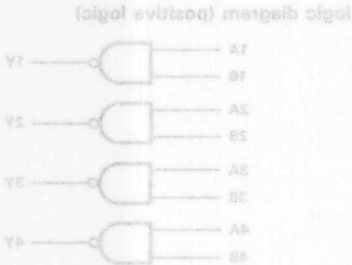
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

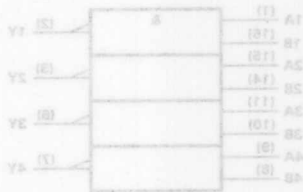
		54ACT11000		74ACT11000		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

2

Advanced CMOS Circuits



OUTPUT Y	INPUTS A B	
	H	H
L	H	L
L	L	H
H	L	L



This symbol is in accordance with ANSI/IEEE Std 81-1984 and IEC Publication 937-13.
Pin numbers shown are for D, J, and N packages.

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54ACT11000, 74ACT11000
QUADRUPL 2-INPUT POSITIVE-NAND GATES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11000		74ACT11000		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μ A	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
V _{OL}	I _{OL} = 50 μ A	4.5 V			0.1	0.1		0.1		V
		5.5 V			0.1	0.1		0.1		
	I _{OL} = 24 mA	4.5 V			0.36	0.5		0.44		
		5.5 V			0.36	0.5		0.44		
	I _{OL} = 50 mA [†]	5.5 V				1.65				
I _I	V _I = V _{CC} or GND	4.5 V								μ A
		5.5 V			± 0.1	± 1		± 1		
	I _{CC}	4.5 V			4	80		40		
		5.5 V								
	ΔI_{CC} [‡]	5.5 V			0.9	1		1		
C _i	V _I = V _{CC} or GND	5 V			3.5					pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics, V_{CC} = 5 V \pm 0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54ACT11000		74ACT11000		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	1.5	7.2	10.9	1.5	13.3	1.5	12.3	ns
t _{PHL}			1.5	5.8	8	1.5	9.5	1.5	8.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate C _L = 50 pF, f = 1 MHz	23	pF

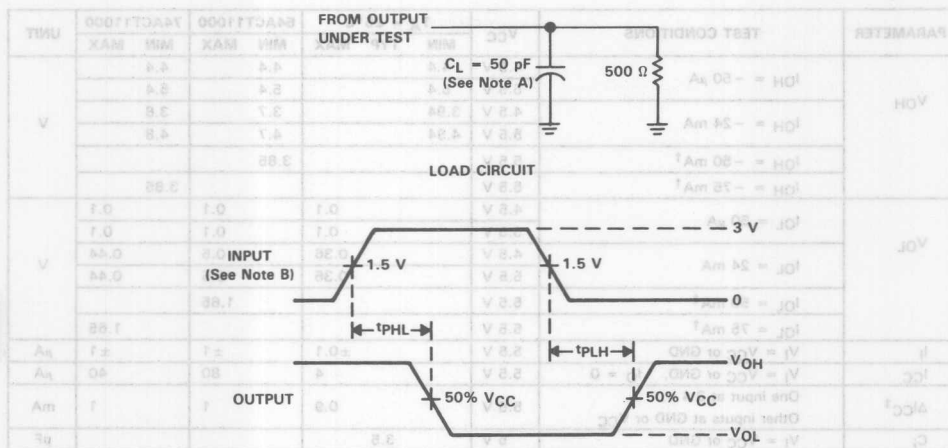
2

Advanced CMOS Circuits

54ACT11000, 74ACT11000 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

2 Advanced CMOS Circuits

PARAMETER MEASUREMENT INFORMATION



PROPAGATION DELAY TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1: LOAD CIRCUIT AND VOLTAGE WAVEFORMS

UNIT	74ACT11000	54ACT11000	PARAMETER	TEST CONDITIONS
ns	12.5	12.5	t_{PLH}	$V_I = V_{CC}$ or GND
ns	8.8	8.8	t_{PLH}	$V_I = V_{CC}$ or GND

operating characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ C$

UNIT	TEST CONDITIONS	PARAMETER
W	$C_L = 50$ pF, $f = 1$ MHz	Power dissipation per gate
W		

54AC11002, 74AC11002 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

D2957, JUNE 1987—REVISED OCTOBER 1987

- New Flow-Through Architecture to Optimize PCB Layout

- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise

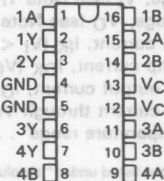
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process

- 500-mA Typical Latch-Up Immunity at 125°C

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

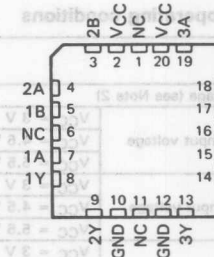
54AC11002 . . . J PACKAGE
74AC11002 . . . D OR N PACKAGE

(TOP VIEW)



54AC11002 . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

description

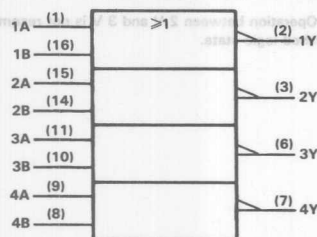
These devices contain four independent 2-input NOR gates. They perform the Boolean functions $Y = A+B$ or $Y = \overline{A+B}$ in positive logic.

The 54AC11002 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74AC11002 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

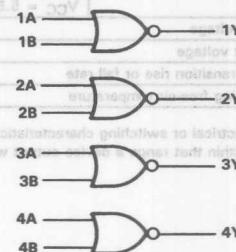
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



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Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11002, 74AC11002 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Storage temperature range	-65°C to 150°C

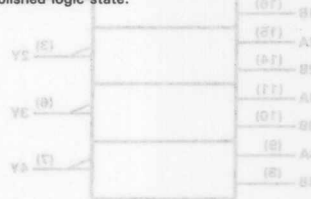
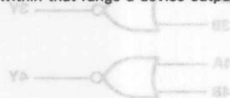
[†]Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54AC11002			74AC11002			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 2)	3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V			2.1			V
		V _{CC} = 4.5 V			3.15			
		V _{CC} = 5.5 V			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V			0.9			V
		V _{CC} = 4.5 V			1.35			
		V _{CC} = 5.5 V			1.65			
I _{OH}	High-level output current	V _{CC} = 3 V			-4			mA
		V _{CC} = 4.5 V			-24			
		V _{CC} = 5.5 V			-24			
I _{OL}	Low-level output current	V _{CC} = 3 V			12			mA
		V _{CC} = 4.5 V			24			
		V _{CC} = 5.5 V			24			
V _I	Input voltage	0	V _{CC}		0	V _{CC}		V
V _O	Output voltage	0	V _{CC}		0	V _{CC}		V
Δt/Δv	Input transition rise or fall rate	0	10		0	10		ns/V
T _A	Operating free-air temperature	-55	125		-40	85		°C

NOTE 2: No electrical or switching characteristics are specified at $V_{CC} < 3$ V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.



This symbol is in accordance with ANSI Std. 91-1984 and IEC Publication 613-13.
Pin numbers shown are for D, J, and H packages.

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2

Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11002, 74AC11002
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11002		74AC11002		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
V _{OL}	I _{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA [†]	5.5 V				1.65				
		5.5 V					1.65			
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		80		40	μA
C _I	V _I = V _{CC} or GND	5 V		3.5						pF

[†]Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C			54AC11002		74AC11002		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	3.3 ± 0.3 V	1.5	7	8.6	1.5	10.7	1.5	9.9	ns
			5 ± 0.5 V	1.5	4.5	6.1	1.5	7.4	1.5	6.9	
t _{PHL}			3.3 ± 0.3 V	1.5	6	7.5	1.5	9	1.5	8.4	
			5 ± 0.5 V	1.5	4	5.7	1.5	6.8	1.5	6.4	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per gate	C _L = 50 pF, f = 1 MHz	32	pF

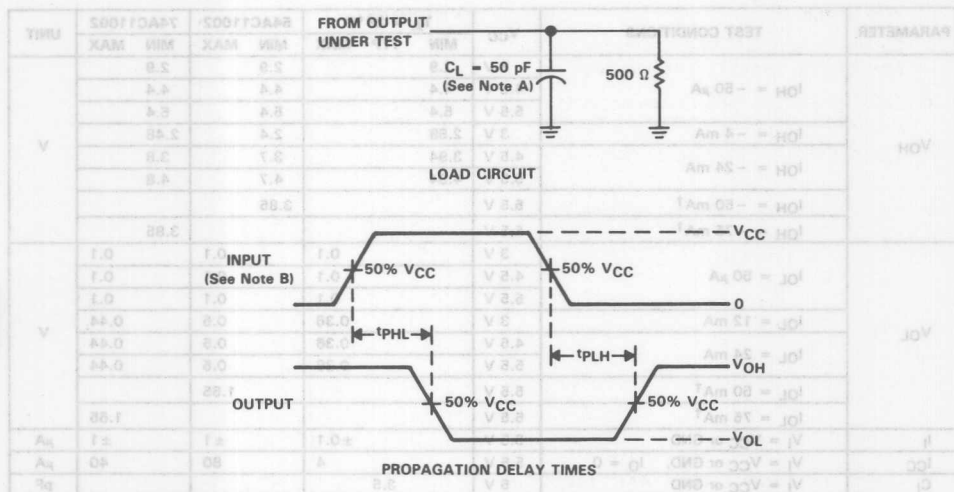
2

Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11002, 74AC11002 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_0 = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 - C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC RANGE	$T_A = 25^\circ\text{C}$			
				MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$2.3 \pm 0.3 \text{ V}$	1.8	3	8.8	ns
			$2.4 \pm 0.3 \text{ V}$	1.8	4.8	8.7	ns
t_{PLH}	A or B	Y	$2.3 \pm 0.3 \text{ V}$	1.8	8	7.8	ns
			$2.4 \pm 0.3 \text{ V}$	1.8	4	8.7	ns

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{PD} Power dissipation capacitance per gate	$C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$	32	ps

2

Advanced CMOS Circuits

PRODUCT PREVIEW

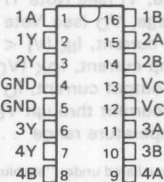
54ACT11002, 74ACT11002 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

D2957, JUNE 1987

- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

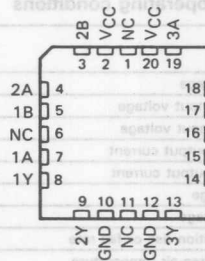
54ACT11002 ... J PACKAGE
74ACT11002 ... D OR N PACKAGE

(TOP VIEW)



54ACT11002 ... FK PACKAGE

(TOP VIEW)



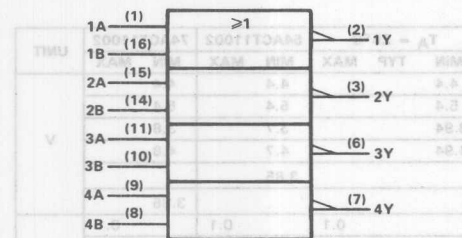
NC—No internal connection

description

These devices contain four independent 2-input NOR gates. They perform the Boolean functions $Y = A+B$ or $Y = A+B$ in positive logic.

The 54ACT11002 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11002 is characterized for operation from -40°C to 85°C.

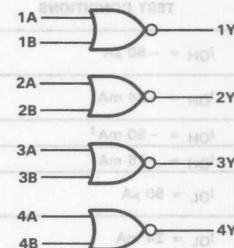
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

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54ACT11002, 74ACT11002 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Storage temperature range	-65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11002		74ACT11002		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		-24		-24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta V$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			54ACT11002		74ACT11002		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	$I_{OH} = -50 \text{ mA}^\ddagger$	5.5 V				3.85				
V_{OL}	$I_{OL} = 50 \mu\text{A}$	4.5 V		0.1		0.1		0.1		V
		5.5 V		0.1		0.1		0.1		
	$I_{OL} = 24 \text{ mA}$	4.5 V		0.36		0.5		0.44		
		5.5 V		0.36		0.5		0.44		
	$I_{OL} = 50 \text{ mA}^\ddagger$	5.5 V				1.65				
I_{CC}	$V_I = V_{CC}$ or GND	5.5 V		± 0.1		± 1		± 1		μA
	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		4		80		40		
ΔI_{CC}^\S	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V		0.9		1		1		mA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5						pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

2

Advanced CMOS Circuits

54ACT11002, 74ACT11002 QUADRUPL 2-INPUT POSITIVE-NOR GATES

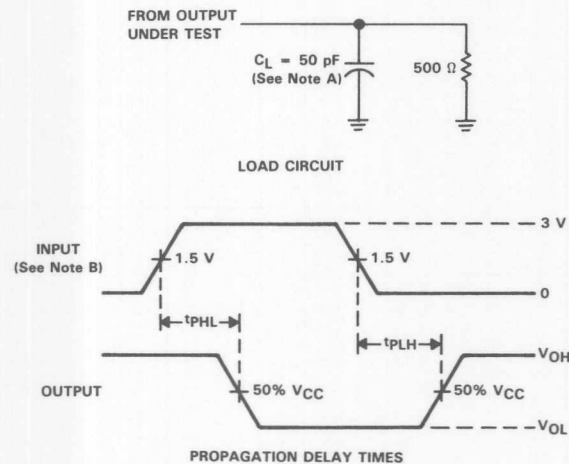
switching characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11002		74ACT11002		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	6.1	9.4	1.5	11.3	1.5	10.6	ns
t_{PHL}			1.5	5.3	7.8	1.5	9.3	1.5	8.7	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per gate	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	29	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

switching characteristics, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$				UNIT
			MIN	TYP	MAX	MIN	
Y ₀₁	A or B	Y	1.5	0.1	0.4	1.5	ns
			1.5	0.3	0.5	1.5	
Y ₀₂	A or B	Y	1.5	0.1	0.4	1.5	ns
			1.5	0.3	0.5	1.5	

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate $C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$	23	pF

PARAMETER MEASUREMENT INFORMATION

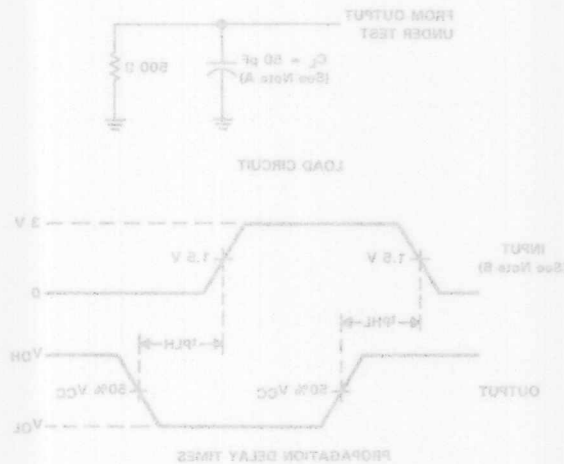


FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

NOTES:
A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $t_r = 50 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. The outputs are measured one at a time with one input transition per measurement.

54AC11008, 74AC11008 QUADRUPLE 2-INPUT POSITIVE-AND GATES

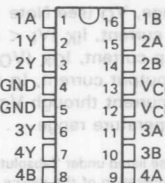
D2957, AUGUST 1987

- New Flow-Through Architecture to Optimize PCB Layout

54AC11008 . . . J PACKAGE

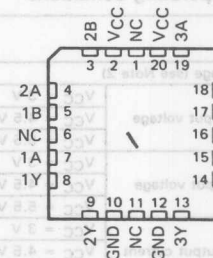
74AC11008 . . . D OR N PACKAGE

(TOP VIEW)



54AC11008 . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise

- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process

- 500-mA Typical Latch-Up Immunity at 125°C

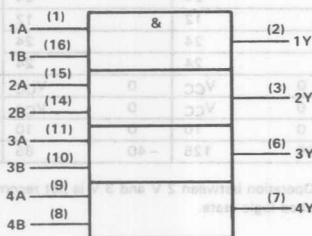
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The 54AC11008 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC11008 is characterized for operation from -40°C to 85°C.

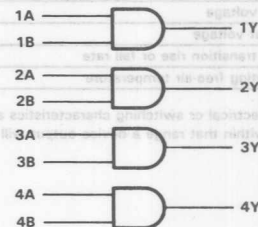
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

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TEXAS
INSTRUMENTS

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2-19

54AC11008, 74AC11008 QUADRUPL 2-INPUT POSITIVE-AND GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	−65°C to 150°C

[†]Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11008			74AC11008			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3$ V	2.1			2.1			V
		$V_{CC} = 4.5$ V	3.15			3.15			
		$V_{CC} = 5.5$ V	3.85			3.85			
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V			0.9			0.9	V
		$V_{CC} = 4.5$ V			1.35			1.35	
		$V_{CC} = 5.5$ V			1.65			1.65	
I_{OH}	High-level output current	$V_{CC} = 3$ V			−4			−4	mA
		$V_{CC} = 4.5$ V			−24			−24	
		$V_{CC} = 5.5$ V			−24			−24	
I_{OL}	Low-level output current	$V_{CC} = 3$ V			12			12	mA
		$V_{CC} = 4.5$ V			24			24	
		$V_{CC} = 5.5$ V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at $V_{CC} < 3$ V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

2

Advanced CMOS Circuits

FUNCTION TABLE (each gate)

INPUTS	OUTPUT
A B	Y
H H	H
L L	L
X X	X

54AC11008, 74AC11008
QUADRUPLE 2-INPUT POSITIVE-AND GATES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11008		74AC11008		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
V _{OL}	I _{OL} = 50 μA	3 V		0.1			0.1		0.1	V
		4.5 V		0.1			0.1		0.1	
		5.5 V		0.1			0.1		0.1	
	I _{OL} = 12 mA	3 V		0.36			0.5		0.44	
		4.5 V		0.36			0.5		0.44	
		5.5 V		0.36			0.5		0.44	
I _I	V _I = V _{CC} or GND	5.5 V		±0.1			±1		±1	μA
	V _I = V _{CC} or GND, I _O = 0	5.5 V		4			80		40	μA
C _i	V _I = V _{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C			54AC11008			74AC11008			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	A or B	Y	3.3 ± 0.3 V	1.5	6.3	9	1.5		11	1.5		10.2	ns
			5 ± 0.5 V	1.5	4.3	6.2	1.5		7.3	1.5		6.9	
t _{PHL}			3.3 ± 0.3 V	1.5	5.6	7.8	1.5		9	1.5		8.6	
			5 ± 0.5 V	1.5	4	5.9	1.5		6.8	1.5		6.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per gate	C _L = 50 pF, f = 1 MHz	29	pF

2 Advanced CMOS Circuits

[illegible]

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_0 = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns
C. The outputs are measured one at a time with one input transition per measurement.

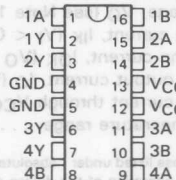
FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54ACT11008, 74ACT11008 QUADRUPLE 2-INPUT POSITIVE-AND GATES

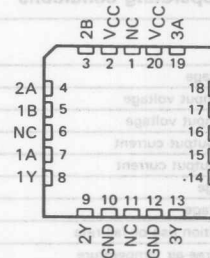
D2957, AUGUST 1987

- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54ACT11008 . . . J PACKAGE
74ACT11008 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11008 . . . FK PACKAGE
(TOP VIEW)

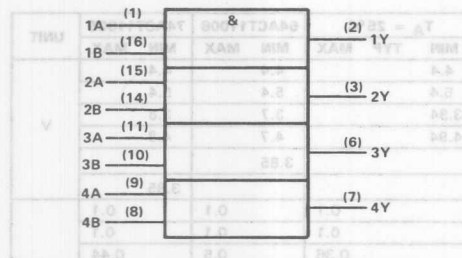


description

These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The 54ACT11008 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11008 is characterized for operation from -40°C to 85°C.

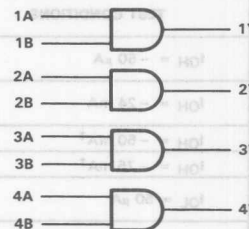
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

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54ACT11008, 74ACT11008 QUADRUPLE 2-INPUT POSITIVE-AND GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC}+0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC}+0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Storage temperature range	-65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11008		74ACT11008		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		-24		-24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			54ACT11008		74ACT11008		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	$I_{OH} = -50 \text{ mA}^\ddagger$	5.5 V				3.85				
V_{OL}	$I_{OL} = 50 \mu\text{A}$	4.5 V		0.1		0.1		0.1		V
		5.5 V		0.1		0.1		0.1		
	$I_{OL} = 24 \text{ mA}$	4.5 V		0.36		0.5		0.44		
		5.5 V		0.36		0.5		0.44		
	$I_{OL} = 50 \text{ mA}^\ddagger$	5.5 V				1.65				
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V								μA
		5.5 V								
ΔI_{CC}^\S	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V		0.9		1		1		mA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5						pF

‡Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

54ACT11008, 74ACT11008 QUADRUPLE 2-INPUT POSITIVE-AND GATES

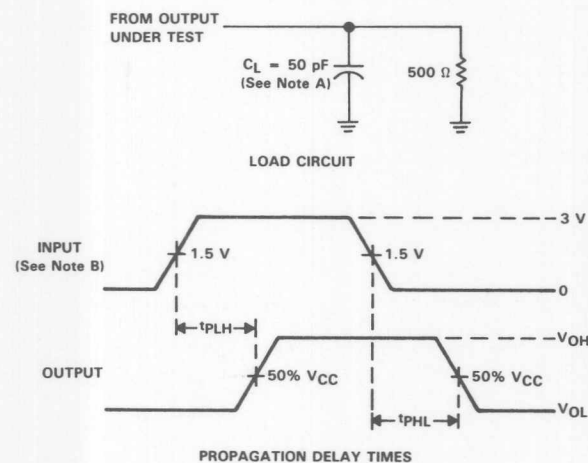
switching characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11008		74ACT11008		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	5.8	8	1.5	9.4	1.5	9	ns
t_{PHL}			1.5	5.2	7.7	1.5	8.6	1.5	8.2	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per gate	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	29	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_0 = 50\text{ }\Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.

C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

switching characteristics, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			
			MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	1.5	2.0	5	ns
			1.5	2.2	5.7	ns
t _{PHL}	A or B	Y	1.5	2.0	5	ns
			1.5	2.2	5.7	ns

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	
C _{pd}	Power dissipation capacitance per gate	$C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$	
		TYP	20 pF

PARAMETER MEASUREMENT INFORMATION

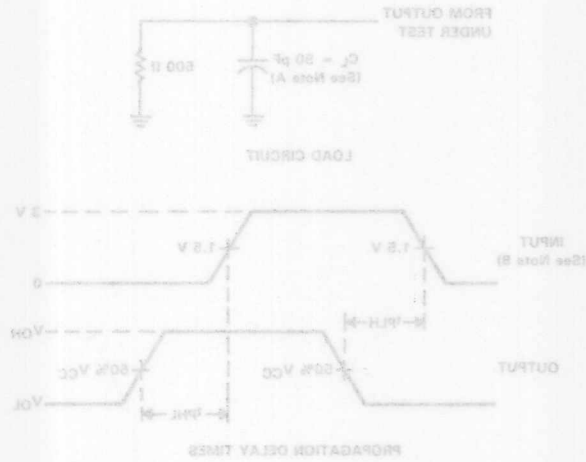


FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

NOTE: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $t_r = 50 \text{ pF}$, $t_f = 3 \text{ ns}$, $r = 3 \text{ ns}$.
C. The output is measured one bit time with one input transition for measurement.

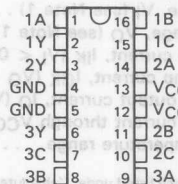
54AC11010, 74AC11010 TRIPLE 3-INPUT POSITIVE-NAND GATES

D2957, MAY 1987

- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

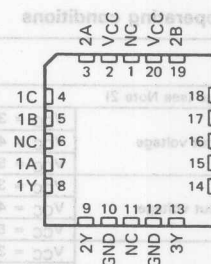
54AC11010 ... J PACKAGE
74AC11010 ... D OR N PACKAGE

(TOP VIEW)



54AC11010 ... FK PACKAGE

(TOP VIEW)

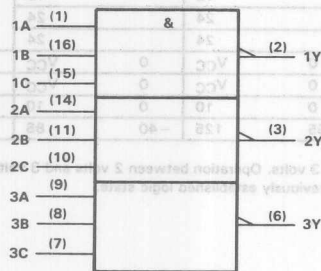


description

These devices contain three independent 3-input NAND gates. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{A + B + C}$ in positive logic.

The 54AC11010 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC11010 is characterized for operation from -40°C to 85°C.

logic symbol†



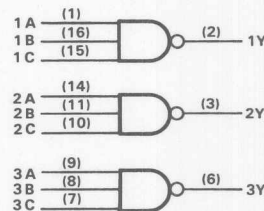
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic diagram (positive logic)



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54AC11010, 74AC11010
TRIPLE 3-INPUT POSITIVE-NAND GATES

54AC11010, 74AC11010

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Storage temperature range	-65°C to 150°C

[†]Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

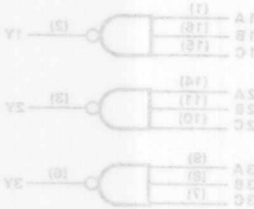
recommended operating conditions

		54AC11010			74AC11010			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 2)	3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V			2.1			V
		V _{CC} = 4.5 V			3.15			
		V _{CC} = 5.5 V			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V			0.9			V
		V _{CC} = 4.5 V			1.35			
		V _{CC} = 5.5 V			1.65			
I _{OH}	High-level output current	V _{CC} = 3 V			-4			mA
		V _{CC} = 4.5 V			-24			
		V _{CC} = 5.5 V			-24			
I _{OL}	Low-level output current	V _{CC} = 3 V			12			mA
		V _{CC} = 4.5 V			24			
		V _{CC} = 5.5 V			24			
V _I	Input voltage	0			V _{CC}			V
V _O	Output voltage	0			V _{CC}			V
Δt/Δv	Input transition rise or fall rate	0			10			ns/V
T _A	Operating free-air temperature	-55			125			°C
		-40			85			

NOTE 2: No electrical or switching characteristics are specified at V_{CC} less than 3 volts. Operation between 2 volts and 3 volts is not recommended, but within that range, a device output will maintain a previously established logic state.

2

Advanced CMOS Circuits



54AC11010, 74AC11010
TRIPLE 3-INPUT POSITIVE-NAND GATES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11010		74AC11010		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
	I _{OH} = -24 mA	5.5 V	4.94			4.7		4.8		
V _{OL}	I _{OL} = 50 µA	3 V			0.1	0.1		0.1		V
		4.5 V			0.1	0.1		0.1		
		5.5 V			0.1	0.1		0.1		
	I _{OL} = 12 mA	3 V			0.36	0.5		0.44		
		4.5 V			0.36	0.5		0.44		
	I _{OL} = 24 mA	5.5 V			0.36	0.5		0.44		
	I _{OL} = 50 mA†	5.5 V				1.65				
	I _{OL} = 75 mA†	5.5 V						1.65		
I _I	V _I = V _{CC} or GND	5.5 V			±0.1	±1		±1		µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4	80		40		µA
C _i	V _I = V _{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics (see Figure 1 for load circuits and waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C			54AC11010		74AC11010		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	ANY	Y	3.3 V ± 0.3 V	1.5	5.9	8.5	1.5	10	1.5	9.3	ns
			5 V ± 0.5 V	1.5	4.4	6.2	1.5	7.1	1.5	6.7	
t _{PHL}			3.3 V ± 0.3 V	1.5	5.8	9	1.5	10.4	1.5	9.9	ns
			5 V ± 0.5 V	1.5	4.6	6.4	1.5	7.4	1.5	7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per gate	C _L = 50 pF, f = 1 MHz	23	pF

2

Advanced CMOS Circuits

2 Advanced CMOS Circuits

PARAMETER MEASUREMENT INFORMATION

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_o = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
C. The outputs are measured one at a time with one input transition per measurement.

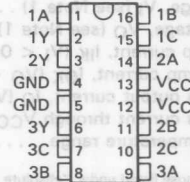
UNIT	TRANSISTOR	DIODE	SWITCH	V _{CE} RANGE	TO (OUTPUT)	FROM (INPUT)	PARAMETER
10	MIN MAX	MIN MAX	MIN TYP MAX	3.0 V ± 0.5 V	Y	ANY	P ₁
10	1.5 2.5	1.5 10	1.5 8.0 8.5	3.0 V ± 0.5 V			
10	1.5 8.5	1.5 7.1	1.5 4.4 8.2	3.0 V ± 0.5 V			
10	1.5 8.5	1.5 10.4	1.5 8.5 9	3.0 V ± 0.5 V	Y	ANY	P ₂
10	1.5 8.5	1.5 7.4	1.5 4.5 8.4	3.0 V ± 0.5 V			
10	1.5 8.5	1.5 7.4	1.5 4.5 8.4	3.0 V ± 0.5 V			

54ACT11010, 74ACT11010 TRIPLE 3-INPUT POSITIVE-NAND GATES

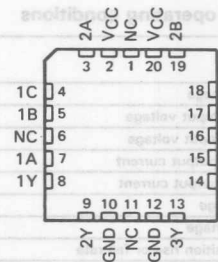
D2957, JULY 1987

- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54ACT11010 ... J PACKAGE
74ACT11010 ... D OR N PACKAGE
(TOP VIEW)



54ACT11010 ... FK PACKAGE
(TOP VIEW)



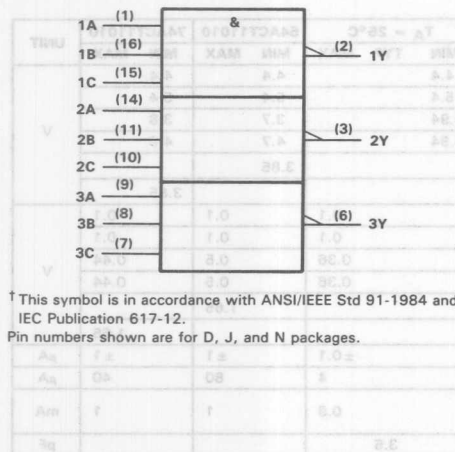
NC—No internal connection

description

These devices contain three independent 3-input NAND gates. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{A + B + C}$ in positive logic.

The 54ACT11010 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11010 is characterized for operation from -40°C to 85°C.

logic symbol†



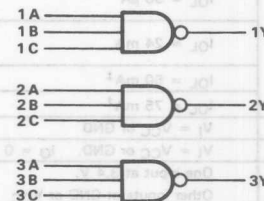
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

FUNCTION TABLE
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic diagram (positive logic)



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TEXAS
INSTRUMENTS

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54ACT11010, 74ACT11010

TRIPLE 3-INPUT POSITIVE-NAND GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11010		74ACT11010		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		-24		-24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			54ACT11010		74ACT11010		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	$I_{OH} = -50 \text{ mA}^\dagger$	5.5 V				3.85				
V_{OL}	$I_{OL} = 50 \mu\text{A}$	4.5 V		0.1		0.1		0.1		V
		5.5 V		0.1		0.1		0.1		
	$I_{OL} = 24 \text{ mA}$	4.5 V		0.36		0.5		0.44		
		5.5 V		0.36		0.5		0.44		
	$I_{OL} = 50 \text{ mA}^\dagger$	5.5 V				1.65				
I_I	$V_I = V_{CC}$ or GND	5.5 V		± 0.1		± 1		± 1		μA
	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		4		80		40		μA
ΔI_{CC}^\ddagger	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V		0.9		1		1		mA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

2

Advanced CMOS Circuits

54ACT11010, 74ACT11010 TRIPLE 3-INPUT POSITIVE-NAND GATES

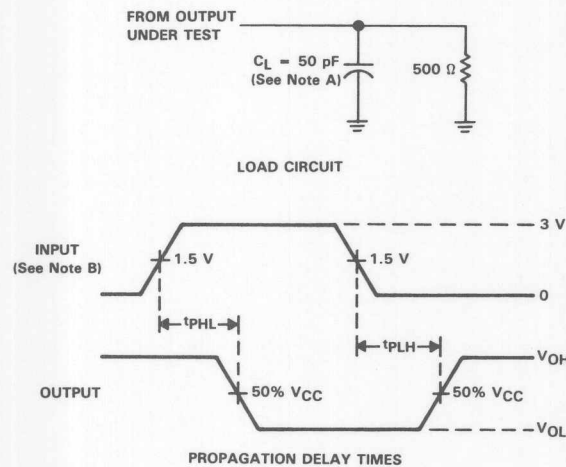
switching characteristics, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11010		74ACT11010		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	5.8	8.2	1.5	9.3	1.5	8.9	ns
t_{PHL}			1.5	5.7	7.4	1.5	8.7	1.5	8.2	

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per gate	$C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$	27	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.

C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54AC11011, 74AC11011 TRIPLE 3-INPUT POSITIVE-AND GATES

D2957, JULY 1987

- New Flow-Through Architecture to Optimize PCB Layout

- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise

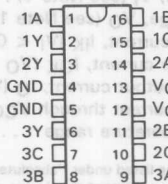
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process

- 500-mA Typical Latch-Up Immunity at 125°C

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

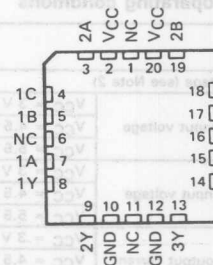
54AC11011 . . . J PACKAGE
74AC11011 . . . D OR N PACKAGE

(TOP VIEW)



54AC11011 . . . FK PACKAGE

(TOP VIEW)



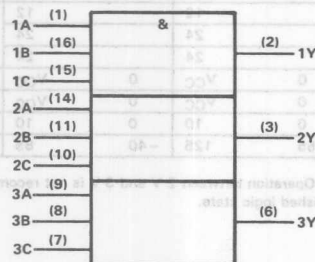
NC—No internal connection

description

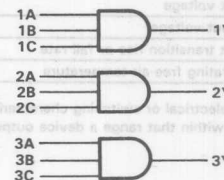
These devices contain three independent 3-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{A + B + C}$ in positive logic.

The 54AC11011 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74AC11011 is characterized for operation from -40°C to 85°C .

logic symbol†



logic diagram (positive logic)



FUNCTION TABLE (each gate)

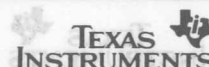
INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

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Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11011, 74AC11011

TRIPLE 3-INPUT POSITIVE-AND GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) †

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	−65°C to 150°C

†Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54AC11011			74AC11011			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)	3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3$ V		2.1	$V_{CC} = 3$ V		2.1	V
		$V_{CC} = 4.5$ V		3.15	$V_{CC} = 4.5$ V		3.15	
		$V_{CC} = 5.5$ V		3.85	$V_{CC} = 5.5$ V		3.85	
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V		0.9	$V_{CC} = 3$ V		0.9	V
		$V_{CC} = 4.5$ V		1.35	$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 5.5$ V		1.65	$V_{CC} = 5.5$ V		1.65	
I_{OH}	High-level output current	$V_{CC} = 3$ V		−4	$V_{CC} = 3$ V		−4	mA
		$V_{CC} = 4.5$ V		−24	$V_{CC} = 4.5$ V		−24	
		$V_{CC} = 5.5$ V		−24	$V_{CC} = 5.5$ V		−24	
I_{OL}	Low-level output current	$V_{CC} = 3$ V		12	$V_{CC} = 3$ V		12	mA
		$V_{CC} = 4.5$ V		24	$V_{CC} = 4.5$ V		24	
		$V_{CC} = 5.5$ V		24	$V_{CC} = 5.5$ V		24	
V_I	Input voltage	0	V_{CC}	0	0	V_{CC}	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	0	V_{CC}	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	0	10	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85			°C

NOTE 2: No electrical or switching characteristics are specified at $V_{CC} < 3$ V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

INPUTS		OUTPUT
A	B	
H	H	H
L	X	L
X	L	X
X	X	X

54AC11011, 74AC11011
TRIPLE 3-INPUT POSITIVE-AND GATES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11011			74AC11011			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 µA	3 V	2.9			2.9			2.9			V
		4.5 V	4.4			4.4			4.4			
		5.5 V	5.4			5.4			5.4			
	I _{OH} = -4 mA	3 V	2.58			2.4			2.48			
		4.5 V	3.94			3.7			3.8			
	I _{OH} = -24 mA	5.5 V	4.94			4.7			4.8			
		5.5 V				3.85			3.85			
V _{OL}	I _{OL} = 50 µA	3 V		0.1		0.1			0.1			V
		4.5 V		0.1		0.1			0.1			
		5.5 V		0.1		0.1			0.1			
	I _{OL} = 12 mA	3 V		0.36		0.5			0.44			
		4.5 V		0.36		0.5			0.44			
	I _{OL} = 24 mA	5.5 V		0.36		0.5			0.44			
		5.5 V				1.65			1.65			
I _I	V _I = V _{CC} or GND	5.5 V		±0.1		±1			±1			µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		4		80			40			µA
C _i	V _I = V _{CC} or GND	5 V		3.5								pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C			54AC11011			74AC11011			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	Any	Y	3.3 ± 0.3 V										ns
			5 ± 0.5 V		4								
t _{PHL}			3.3 ± 0.3 V										
			5 ± 0.5 V		4.3								

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per gate	C _L = 50 pF, f = 1 MHz	23	pF

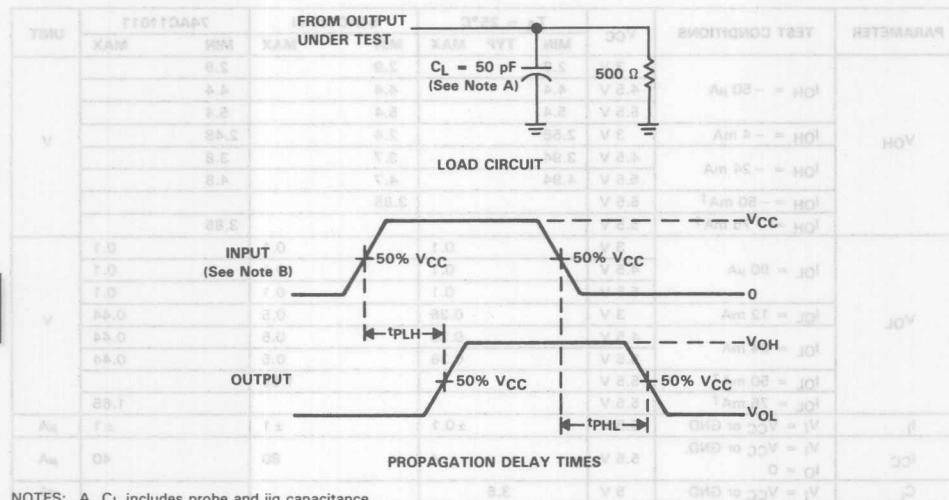
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Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11011, 74AC11011
TRIPLE 3-INPUT POSITIVE-AND GATES

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

PARAMETER	TEST CONDITIONS	UNIT
t_{PLH}	$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$	ns
t_{PHL}	$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$	ns

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	UNIT
C_{in}	$C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$	pf

2

Advanced CMOS Circuits

PRODUCT PREVIEW

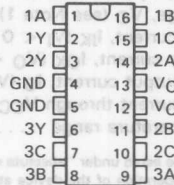
54ACT11011, 74ACT11011 TRIPLE 3-INPUT POSITIVE-AND GATES

D2957, JULY 1987—REVISED NOVEMBER 1987

- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

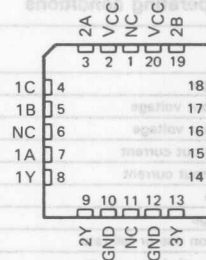
54ACT11011 . . . J PACKAGE
74ACT11011 . . . D OR N PACKAGE

(TOP VIEW)



54ACT11011 . . . FK PACKAGE

(TOP VIEW)

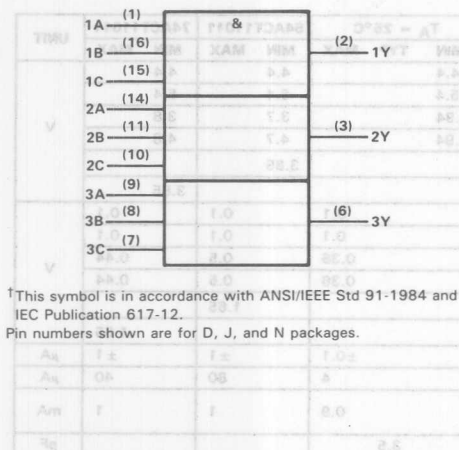


description

These devices contain three independent 3-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The 54ACT11011 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11011 is characterized for operation from -40°C to 85°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

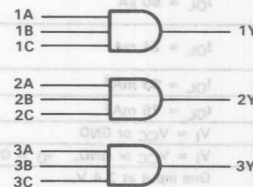
Pin numbers shown are for D, J, and N packages.

NC—No internal connection

FUNCTION TABLE (each gate)

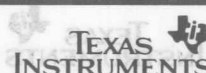
INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic diagram (positive logic)



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54ACT11011, 74ACT11011 TRIPLE 3-INPUT POSITIVE-AND GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	−65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11011		74ACT11011		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			54ACT11011		74ACT11011		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	$I_{OH} = -50 \text{ mA}^\ddagger$	5.5 V				3.85				
V_{OL}	$I_{OL} = 50 \mu\text{A}$	4.5 V		0.1		0.1		0.1		V
		5.5 V		0.1		0.1		0.1		
	$I_{OL} = 24 \text{ mA}$	4.5 V		0.36		0.5		0.44		
		5.5 V		0.36		0.5		0.44		
	$I_{OL} = 50 \text{ mA}^\ddagger$	5.5 V				1.65				
I_{CC}	$V_I = V_{CC}$ or GND	5.5 V			±0.1	±1		±1		μA
	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4	80		40		μA
ΔI_{CC}^\S	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9	1		1		mA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5						pF

‡Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

2

Advanced CMOS Circuits

54ACT11011, 74ACT11011 TRIPLE 3-INPUT POSITIVE-AND GATES

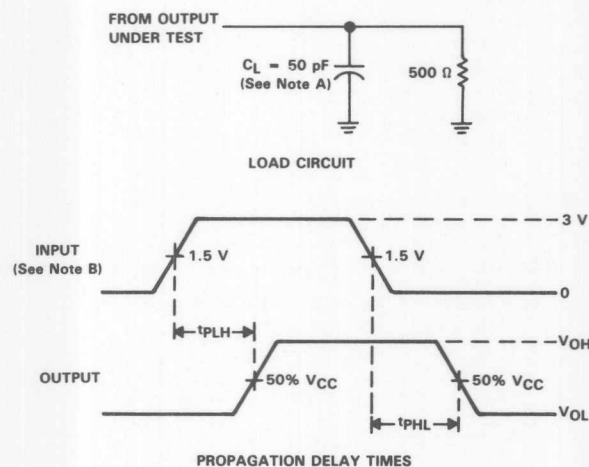
switching characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11011		74ACT11011		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, or C	Y	1.5	6.5	8.6	1.5	10.2	1.5	9.6	ns
t_{PHL}			1.5	5.5	7.9	1.5	9.2	1.5	8.7	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per gate	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	28	pF

PARAMETER MEASUREMENT INFORMATION

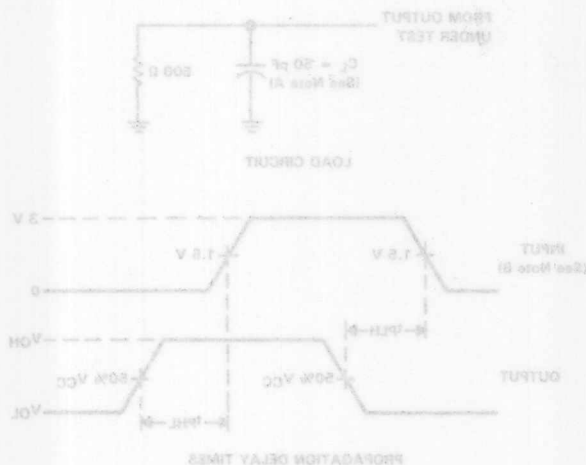


NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_0 = 50\text{ }\Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

FIGURE 7. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generator having the following characteristics: PRR = 10 MHz, $Z_0 = 50 \Omega$, $V_p = 3$ V.
C. The outputs are measured one at a time with one input transition per measurement.



PARAMETER MEASUREMENT INFORMATION

PARAMETER	TEST CONDITIONS	UNIT
C_{PD} Power dissipation capacitance per gate	$C_L = 50$ pF, $f = 1$ MHz	pF
	TYP	28

operating characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$	54ACT11011	74ACT11011	UNIT
PROP	A, B, or C	Y	1.5	8.5	7.5	ns
			1.5	8.5	7.5	ns
T _{PLH}	A, B, or C	Y	1.5	8.5	7.5	ns
			1.5	8.5	7.5	ns

switching characteristics, $V_{CC} = 5$ V ± 0.5 V (see Figure 7)

TRIPLE 3-INPUT POSITIVE-AND GATES
54ACT11011, 74ACT11011

54AC11020, 74AC11020 DUAL 4-INPUT POSITIVE-NAND GATES

D2957, MARCH 1987

- New Flow-Through Architecture to Optimize PCB Layout

- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise

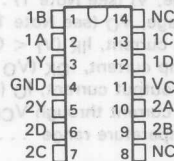
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process

- 500-mA Typical Latch-Up Immunity at 125°C

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

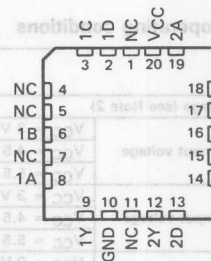
54AC11020 . . . J PACKAGE
74AC11020 . . . D OR N PACKAGE

(TOP VIEW)



54AC11020 . . . FK PACKAGE

(TOP VIEW)

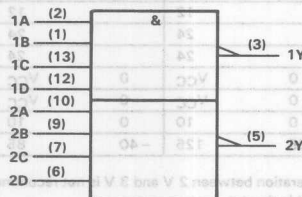


description

These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{A + B + C + D}$ in positive logic.

The 54AC11020 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74AC11020 is characterized for operation from -40°C to 85°C .

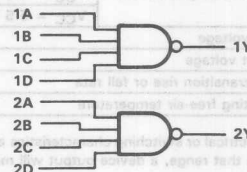
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



FUNCTION TABLE (each gate)

INPUTS				OUTPUT Y
A	B	C	D	
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

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54AC11020, 74AC11020 DUAL 4-INPUT POSITIVE-NAND GATES

1987 HUMAN 7883C

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	−65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54AC11020			74AC11020			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 2)	3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V			2.1			V
		V _{CC} = 4.5 V			3.15			
		V _{CC} = 5.5 V			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V			0.9			V
		V _{CC} = 4.5 V			1.35			
		V _{CC} = 5.5 V			1.65			
I _{OH}	High-level output current	V _{CC} = 3 V			−4			mA
		V _{CC} = 4.5 V			−24			
		V _{CC} = 5.5 V			−24			
I _{OL}	Low-level output current	V _{CC} = 3 V			12			mA
		V _{CC} = 4.5 V			24			
		V _{CC} = 5.5 V			24			
V _I	Input voltage	0		V _{CC}	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise or fall rate	0		10	0		10	ns/V
T _A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at $V_{CC} < 3$ V. Operation between 2 V and 3 V is not recommended, but within that range, a device output will maintain a previously established logic state.

FUNCTION TABLE (each gate)

OUTPUT Y	INPUTS			
	A	B	C	D
L	H	H	H	H
H	L	X	X	X
H	X	L	X	X
H	X	X	L	X
H	X	X	X	L

54AC11020, 74AC11020
DUAL 4-INPUT POSITIVE-NAND GATES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11020		74AC11020		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
	I _{OH} = -24 mA	5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA†	5.5 V				3.85				
V _{OL}	I _{OL} = 50 µA	3 V		0.1		0.1		0.1		V
		4.5 V		0.1		0.1		0.1		
		5.5 V		0.1		0.1		0.1		
	I _{OL} = 12 mA	3 V		0.36		0.5		0.44		
		4.5 V		0.36		0.5		0.44		
	I _{OL} = 24 mA	5.5 V		0.36		0.5		0.44		
	I _{OL} = 50 mA†	5.5 V				1.65				
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4	80		40		µA
		5 V			3.5					pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 milliseconds.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C			54AC11020		74AC11020		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	Any	Y	3.3 ± 0.3 V	1.5	6.4	8.6	1.5	10	1.5	9.4	ns
			5 ± 0.5 V	1.5	4.3	6.3	1.5	7	1.5	6.7	
t _{PHL}			3.3 ± 0.3 V	1.5	6.4	9.2	1.5	10.7	1.5	10.1	
			5 ± 0.5 V	1.5	4.4	6.7	1.5	7.7	1.5	7.3	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per gate	C _L = 50 pF, f = 1 MHz	19	pF

2

PARAMETER MEASUREMENT INFORMATION

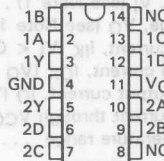
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_0 = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
C. The outputs are measured one at a time with one input transition per measurement.

54ACT11020, 74ACT11020 DUAL 4-INPUT POSITIVE-NAND GATES

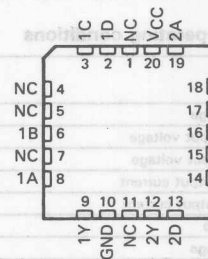
D2957, JUNE 1987

- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54ACT11020 ... J PACKAGE
74ACT11020 ... D OR N PACKAGE
(TOP VIEW)



54ACT11020 ... FK PACKAGE
(TOP VIEW)



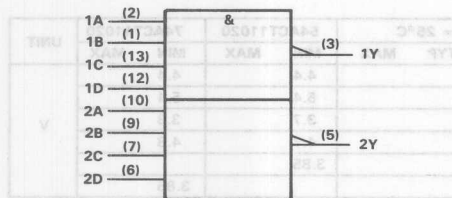
NC—No internal connection

description

These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$ in positive logic.

The 54ACT11020 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74ACT11020 is characterized for operation from -40°C to 85°C .

logic symbol†



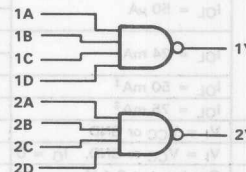
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic diagram (positive logic)



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54ACT11020, 74ACT11020 DUAL 4-INPUT POSITIVE-NAND GATES

TEST DATA

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	–0.5 V to 7 V
Input voltage, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	–65°C to 150°C

[†]Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11020		74ACT11020		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		–24		–24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			54ACT11020		74ACT11020		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	$I_{OH} = -50 \text{ mA}^\dagger$	5.5 V				3.85				
V_{OL}	$I_{OL} = 50 \mu\text{A}$	4.5 V		0.1		0.1		0.1		V
		5.5 V		0.1		0.1		0.1		
	$I_{OL} = 24 \text{ mA}$	4.5 V		0.36		0.5		0.44		
		5.5 V		0.36		0.5		0.44		
	$I_{OL} = 50 \text{ mA}^\dagger$	5.5 V				1.65				
	$I_{OL} = 75 \text{ mA}^\dagger$	5.5 V						1.65		
I_I	$V_I = V_{CC}$ or GND	5.5 V		±0.1		±1		±1		μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		4		80		40		μA
ΔI_{CC}^\S	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V		0.9		1		1		mA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5						pF

[†]Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[§]This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

2

Advanced CMOS Circuits

54ACT11020, 74ACT11020 DUAL 4-INPUT POSITIVE-NAND GATES

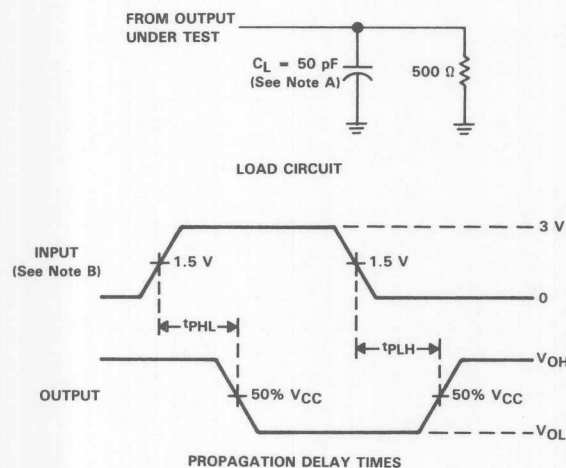
switching characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11020		74ACT11020		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	5.6	8.5	1.5	9.5	1.5	9.1	ns
t_{PHL}			1.5	6.1	8.4	1.5	9.8	1.5	9.2	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per gate	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	27	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\text{ }\Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54AC11021, 74AC11021 DUAL 4-INPUT POSITIVE-AND GATES

D2957, JULY 1987

- New Flow-Through Architecture to Optimize PCB Layout

- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise

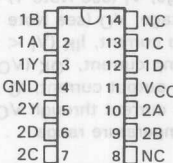
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process

- 500-mA Typical Latch-Up Immunity at 125°C

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

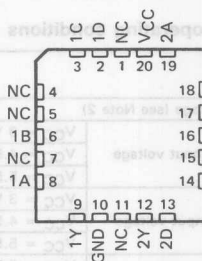
54AC11021 . . . J PACKAGE
74AC11021 . . . D OR N PACKAGE

(TOP VIEW)



54AC11021 . . . FK PACKAGE

(TOP VIEW)



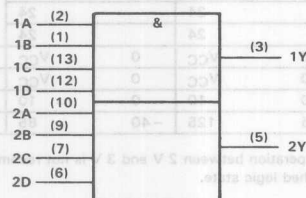
NC—No internal connection

description

These devices contain two independent 4-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{A + B + C + D}$ in positive logic.

The 54AC11021 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74AC11021 is characterized for operation from -40°C to 85°C .

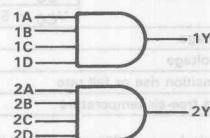
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

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TEXAS
INSTRUMENTS

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Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11021, 74AC11021

DUAL 4-INPUT POSITIVE-AND GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	–0.5 V to 7 V
Input voltage, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	–65°C to 150°C

[†]Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11021			74AC11021			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1			2.1			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 5.5 V	3.85			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V							V
		V _{CC} = 4.5 V	0.9			0.9			
		V _{CC} = 5.5 V	1.35			1.35			
I _{OH}	High-level output current	V _{CC} = 3 V							mA
		V _{CC} = 4.5 V	1.65			1.65			
		V _{CC} = 5.5 V	-4			-4			
I _{OL}	Low-level output current	V _{CC} = 3 V							mA
		V _{CC} = 4.5 V	-24			-24			
		V _{CC} = 5.5 V	12			12			
V _I	Input voltage		0			V _{CC}			V
V _O	Output voltage		0			V _{CC}			V
Δt/Δv	Input transition rise or fall rate		0			10			ns/V
T _A	Operating free-air temperature		-55			125			°C

NOTE 2: No electrical or switching characteristics are specified at $V_{CC} < 3$ V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

OUTPUT	INPUTS			
	A	B	C	D
H	H	H	H	H
L	X	X	X	L
L	X	X	L	X
L	X	L	X	X
L	L	X	X	X

2

Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11021, 74AC11021
DUAL 4-INPUT POSITIVE-AND GATES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11021		74AC11021		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
	I _{OH} = -24 mA	5.5 V	4.94			4.7		4.8		
V _{OL}	I _{OL} = 50 µA	3 V		0.1		0.1		0.1		V
		4.5 V		0.1		0.1		0.1		
		5.5 V		0.1		0.1		0.1		
	I _{OL} = 12 mA	3 V		0.36		0.5		0.44		
		4.5 V		0.36		0.5		0.44		
	I _{OL} = 24 mA	5.5 V		0.36		0.5		0.44		
I _I	V _I = V _{CC} or GND	5.5 V		±0.1		±1		±1		µA
	V _I = V _{CC} or GND, I _O = 0	5.5 V				80		40		µA
C _i	V _I = V _{CC} or GND	5 V		3.5						pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

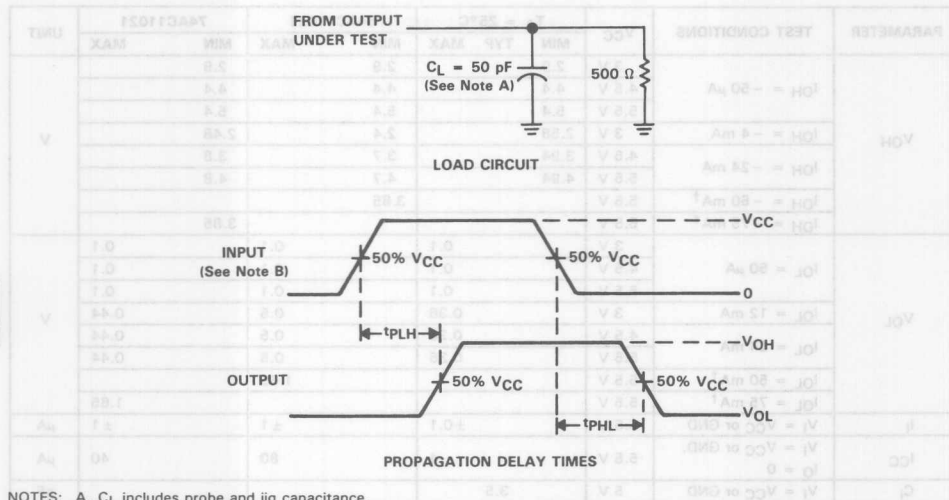
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C			54AC11021		74AC11021		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	Any	Y	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.3						
			3.3 ± 0.3 V								
			5 ± 0.5 V		4.1						

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per gate	C _L = 50 pF, f = 1 MHz	38	pF

54AC11021, 74AC11021
DUAL 4-INPUT POSITIVE-AND GATES

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_0 = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

UNIT	74AC11021		54AC11021		VCC RANGE	TO (OUTPUT)	FROM (INPUT)	PARAMETER
	MAX	MIN	MAX	MIN				
ns					2.3 \pm 0.3 V	Y	Any	t_{PLH}
					2.3 \pm 0.3 V			t_{PHL}
					2.3 \pm 0.3 V			t_{PLH}
					2.3 \pm 0.3 V			t_{PHL}

UNIT	TEST CONDITIONS		PARAMETER
	TYP	MAX	
ns	38	50	t_{PLH}

2

Advanced CMOS Circuits

PRODUCT PREVIEW

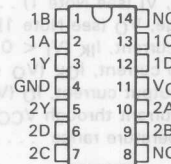
54ACT11021, 74ACT11021 DUAL 4-INPUT POSITIVE-AND GATES

D2957, JULY 1987

- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

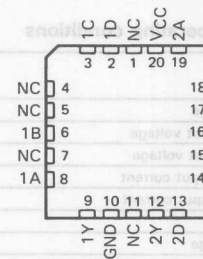
54ACT11021 ... J PACKAGE
74ACT11021 ... D OR N PACKAGE

(TOP VIEW)



54ACT11021 ... FK PACKAGE

(TOP VIEW)



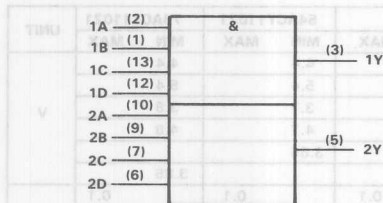
NC—No internal connection

description

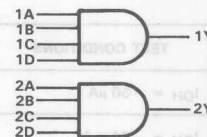
These devices contain two independent 4-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The 54ACT11021 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11021 is characterized for operation from -40°C to 85°C.

logic symbol†



logic diagram (positive logic)



FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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54ACT11021, 74ACT11021
DUAL 4-INPUT POSITIVE-AND GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	−65 °C to 150 °C

[†]Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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Advanced CMOS Circuits

PRODUCT PREVIEW

recommended operating conditions

		54ACT11021		74ACT11021		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t / \Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			54ACT11021		74ACT11021		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50\ \mu\text{A}$	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -24\ \text{mA}$	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	$I_{OH} = -50\ \text{mA}^\ddagger$	5.5 V				3.85				
V_{OL}	$I_{OL} = 50\ \mu\text{A}$	4.5 V		0.1		0.1		0.1		V
		5.5 V		0.1		0.1		0.1		
	$I_{OL} = 24\ \text{mA}$	4.5 V		0.36		0.5		0.44		
		5.5 V		0.36		0.5		0.44		
	$I_{OL} = 50\ \text{mA}^\ddagger$	5.5 V				1.65				
	$I_{OL} = 75\ \text{mA}^\ddagger$	5.5 V						1.65		
I_I	$V_I = V_{CC}$ or GND	5.5 V		±0.1		±1		±1		μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		4		80		40		μA
ΔI_{CC}^\S	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V		0.9		1		1		mA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5						pF

[‡]Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[§]This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

54ACT11021, 74ACT11021
DUAL 4-INPUT POSITIVE-AND GATES

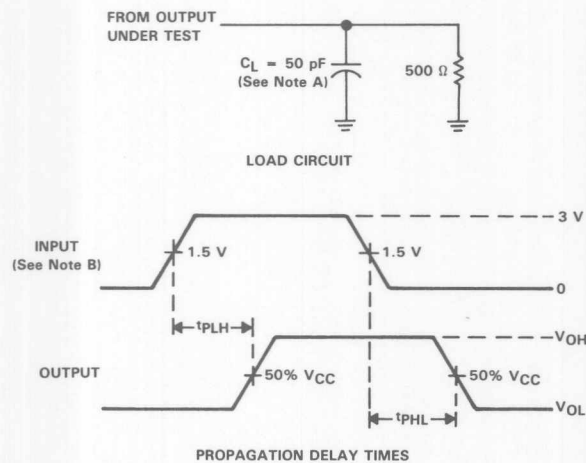
switching characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11021		74ACT11021		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	6.2							ns
t_{PHL}			5							

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per gate	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	37	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.

C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

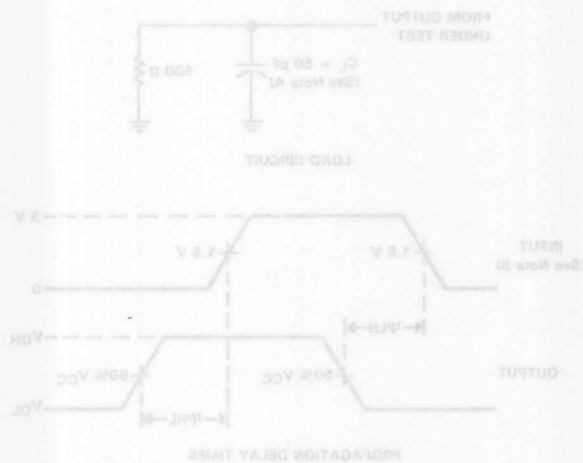
switching characteristics, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$		UNIT
			MIN	MAX	
t_{PLH}	Any	Y	8.5		ns
t_{PHL}			8		

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		UNIT
C_{PD}	Power dissipation capacitance per gate	$C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$	3.3	pF
			TYP	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $P_{DR} \leq 10 \text{ mW}$, $Z_o = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. The outputs are measured one at a time with one input tied to logic 0 for measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54AC11027, 74AC11027 TRIPLE 3-INPUT POSITIVE-NOR GATES

D2957, JULY 1987

- New Flow-Through Architecture to Optimize PCB Layout

- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise

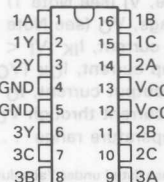
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process

- 500-mA Typical Latch-Up Immunity at 125°C

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

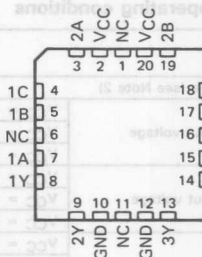
54AC11027 ... J PACKAGE
74AC11027 ... D OR N PACKAGE

(TOP VIEW)



54AC11027 ... FK PACKAGE

(TOP VIEW)



NC—No internal connection

FUNCTION TABLE (each gate)

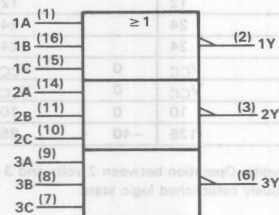
INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

description

These devices contain three independent 3-input NOR gates. They perform the Boolean functions $Y = A+B+C$ or $Y = \bar{A} \cdot \bar{B} \cdot \bar{C}$ in positive logic.

The 54AC11027 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC11027 is characterized for operation from -40°C to 85°C.

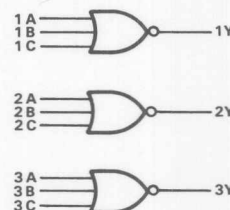
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

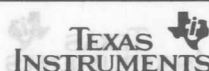
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



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54AC11027, 74AC11027 TRIPLE 3-INPUT POSITIVE-NOR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to $V_{CC}+0.5$ V
Output voltage, V_O (see Note 1)	−0.5 V to $V_{CC}+0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	−65°C to 150°C

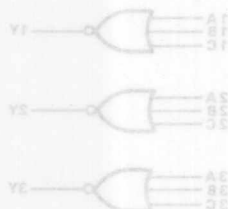
[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		54AC11027			74AC11027			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 2)	3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V			2.1			V
		V _{CC} = 4.5 V			3.15			
		V _{CC} = 5.5 V			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V			0.9			V
		V _{CC} = 4.5 V			1.35			
		V _{CC} = 5.5 V			1.65			
I _{OH}	High-level output current	V _{CC} = 3 V			−4			mA
		V _{CC} = 4.5 V			−24			
		V _{CC} = 5.5 V			−24			
I _{OL}	Low-level output current	V _{CC} = 3 V			12			mA
		V _{CC} = 4.5 V			24			
		V _{CC} = 5.5 V			24			
V _I	Input voltage	0	V _{CC}		0	V _{CC}		V
V _O	Output voltage	0	V _{CC}		0	V _{CC}		V
Δt/Δv	Input transition rise or fall rate	0	10		0	10		ns/V
T _A	Operating free-air temperature	−55	125		−40	85		°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} less than 3 volts. Operation between 2 volts and 3 volts is not recommended, but within that range a device output will maintain a previously established logic state.



54AC11027, 74AC11027
TRIPLE 3-INPUT POSITIVE-NOR GATES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11027		74AC11027		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
	I _{OH} = -24 mA	5.5 V	4.94			4.7		4.8		
		5.5 V				3.85				
V _{OL}	I _{OL} = 50 µA	3 V		0.1		0.1		0.1		V
		4.5 V		0.1		0.1		0.1		
		5.5 V		0.1		0.1		0.1		
	I _{OL} = 12 mA	3 V		0.36		0.5		0.44		
		4.5 V		0.36		0.5		0.44		
	I _{OL} = 24 mA	5.5 V		0.36		0.5		0.44		
		5.5 V				1.65				
I _I	V _I = V _{CC} or GND	5.5 V		±0.1		±1		±1		µA
		5.5 V		4		80		40		µA
C _i	V _I = V _{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25 °C			54AC11027		74AC11027		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	ANY	Y	3.3 V ± 0.3 V	1.5	6.3	9.8	1.5	11.7	1.5	10.9	ns
			5 V ± 0.5 V	1.5	4.3	6.8	1.5	8.1	1.5	7.7	
t _{PHL}			3.3 V ± 0.3 V	1.5	7.6	10.9	1.5	12.9	1.5	12	ns
			5 V ± 0.5 V	1.5	4.5	7.5	1.5	8.9	1.5	8.1	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

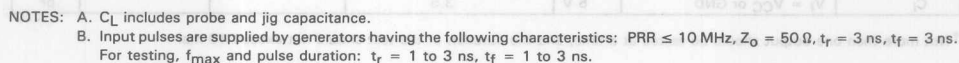
PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per gate	C _L = 50 pF, f = 1 MHz,	24	pF

2

Advanced CMOS Circuits

2 Advanced CMOS Circuits

PARAMETER MEASUREMENT INFORMATION

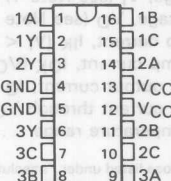


54ACT11027, 74ACT11027 TRIPLE 3-INPUT POSITIVE-NOR GATES

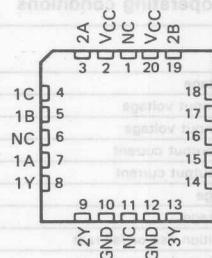
D2957, JULY 1987

- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54ACT11027 . . . J PACKAGE
74ACT11027 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11027 . . . FK PACKAGE
(TOP VIEW)



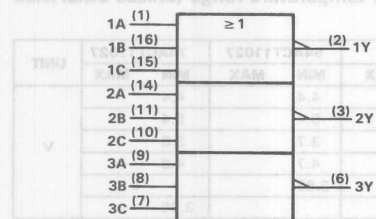
NC—No internal connection

description

These devices contain three independent 3-input NOR gates. They perform the Boolean functions $Y = A + B + C$ or $Y = A \cdot B \cdot C$ in positive logic.

The 54ACT11027 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74ACT11027 is characterized for operation from -40°C to 85°C .

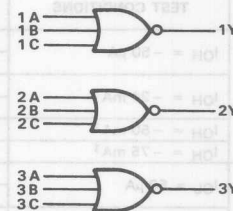
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

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Advanced CMOS Circuits

54ACT11027, 74ACT11027

TRIPLE 3-INPUT POSITIVE-NOR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	–0.5 V to 7 V
Input voltage, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	–65°C to 150°C

[†]Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11027		74ACT11027		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		–24		–24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			54ACT11027		74ACT11027		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	$I_{OH} = -50 \text{ mA}^\ddagger$	5.5 V				3.85				
	$I_{OH} = -75 \text{ mA}^\ddagger$	5.5 V						3.85		
V_{OL}	$I_{OL} = 50 \mu\text{A}$	4.5 V		0.1		0.1		0.1		V
		5.5 V		0.1		0.1		0.1		
	$I_{OL} = 24 \text{ mA}$	4.5 V		0.36		0.5		0.44		
		5.5 V		0.36		0.5		0.44		
	$I_{OL} = 50 \text{ mA}^\ddagger$	5.5 V				1.65				
	$I_{OL} = 75 \text{ mA}^\ddagger$	5.5 V						1.65		
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5 V			4		80		40	μA
ΔI_{CC}^\S	One input at 3.4 V; Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5						pF

[‡]Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[§]This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

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Advanced CMOS Circuits

54ACT11027, 74ACT11027 TRIPLE 3-INPUT POSITIVE-NOR GATES

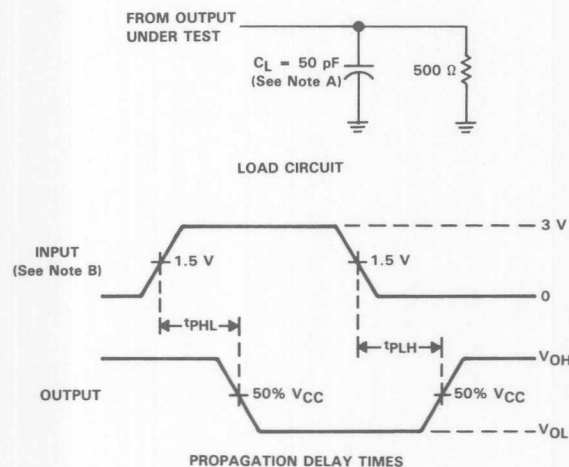
switching characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11027		74ACT11027		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	5	9.2	1.5	10.6	1.5	10.1	ns
t_{PHL}			1.5	6	8.6	1.5	10	1.5	9.4	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per gate	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	27	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.

C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54AC11030, 74AC11030 8-INPUT POSITIVE-NAND GATES

D2957, JUNE 1987

- New Flow-Through Architecture to Optimize PCB Layout

- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise

- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process

- 500-mA Typical Latch-Up Immunity at 125°C

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

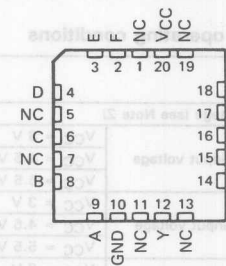
54AC11030 . . . J PACKAGE
74AC11030 . . . D OR N PACKAGE

(TOP VIEW)



54AC11030 . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

description

These devices contain a single 8-input NAND gate and perform the following Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \text{ OR}$$

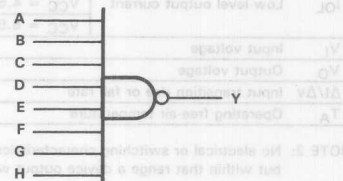
$$Y = \overline{A + B + C + D + E + F + G + H}$$

The 54AC11030 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC11030 is characterized for operation from -40°C to 85°C.

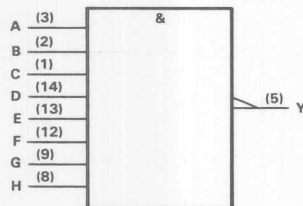
FUNCTION TABLE

INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

logic diagram (positive logic)



logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

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TEXAS
INSTRUMENTS

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54AC11030, 74AC11030 8-INPUT POSITIVE-NAND GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) †

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC}+0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC}+0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Storage temperature range	-65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54AC11030			74AC11030			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 2)	3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V			2.1			V
		V _{CC} = 4.5 V			3.15			
		V _{CC} = 5.5 V			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V			0.9			V
		V _{CC} = 4.5 V			1.35			
		V _{CC} = 5.5 V			1.65			
I _{OH}	High-level output current	V _{CC} = 3 V			-4			mA
		V _{CC} = 4.5 V			-24			
		V _{CC} = 5.5 V			-24			
I _{OL}	Low-level output current	V _{CC} = 3 V			12			mA
		V _{CC} = 4.5 V			24			
		V _{CC} = 5.5 V			24			
V _I	Input voltage	0		V _{CC}	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise or fall rate	0		10	0		10	ns/V
T _A	Operating free-air temperature	-55		125	-40		85	°C

NOTE 2: No electrical or switching characteristics are specified at $V_{CC} < 3$ V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

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Advanced CMOS Circuits

54AC11030, 74AC11030
8-INPUT POSITIVE-NAND GATES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25 °C			54AC11030			74AC11030			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 µA	3 V	2.9			2.9			2.9			V
		4.5 V	4.4			4.4			4.4			
		5.5 V	5.4			5.4			5.4			
	I _{OH} = -4 mA	3 V	2.58			2.4			2.48			
		4.5 V	3.94			3.7			3.8			
		5.5 V	4.94			4.7			4.8			
	I _{OH} = -50 mA [†]	5.5 V				3.85						
V _{OL}	I _{OL} = 50 µA	3 V			0.1			0.1			0.1	V
		4.5 V			0.1			0.1			0.1	
		5.5 V			0.1			0.1			0.1	
	I _{OL} = 12 mA	3 V			0.36			0.5			0.44	
		4.5 V			0.36			0.5			0.44	
		5.5 V			0.36			0.5			0.44	
	I _{OL} = 50 mA [†]	5.5 V						1.65				
I _I	V _I = V _{CC} or GND	5.5 V			±0.1			±1			±1	µA
		5.5 V			4			80			40	µA
C _i	V _I = V _{CC} or GND	5 V			3.5							pF

[†]Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25 °C			54AC11030			74AC11030			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	Any	Y	3.3 ± 0.3 V	1.5	6.9	9.1	1.5		10.6	1.5		9.9	ns
			5 ± 0.5 V	1.5	4.8	6.7	1.5		7.7	1.5		7.2	
t _{PHL}			3.3 ± 0.3 V	1.5	6.4	8.8	1.5		10.6	1.5		9.8	
			5 ± 0.5 V	1.5	4.8	6.7	1.5		8	1.5		7.4	

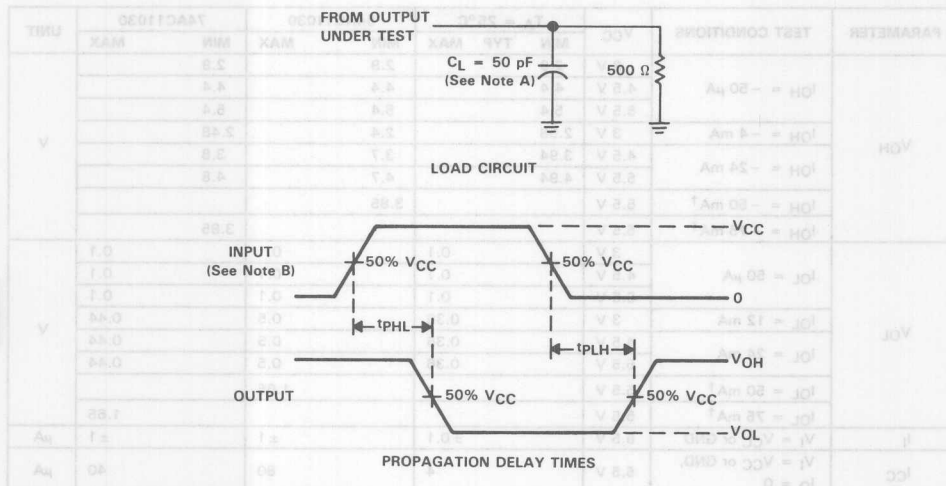
operating characteristics, V_{CC} = 5 V, T_A = 25 °C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per gate	C _L = 50 pF, f = 1 MHz	42	pF

54AC11030, 74AC11030 8-INPUT POSITIVE-NAND GATES

2 Advanced CMOS Circuits

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_0 = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

UNIT	74AC11030		54AC11030		$T_A = 25^\circ\text{C}$		V_{CC}		TO (INPUT)	FROM (OUTPUT)	PARAMETER
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	RANGE			
ns	2.8	1.8	10.8	1.8	8.8	8.1	2.5	$0.3 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$	Y	Any	t_{PLH}
	3.3	1.8	11.1	1.8	8.8	8.1	2.5	$0.3 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$			t_{PHL}
	2.8	1.8	10.8	1.8	8.8	8.1	2.5	$0.3 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$			t_{PLH}
	3.3	1.8	11.1	1.8	8.8	8.1	2.5	$0.3 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$			t_{PHL}

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		UNIT
Power dissipation, $P_{D(ON)}$		$C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$		
Capacitance, C_{in}		$V_{CC} = 5 \text{ V}$, $f = 1 \text{ MHz}$		ps

54ACT11030, 74ACT11030 8-INPUT POSITIVE-NAND GATES

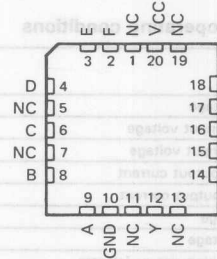
D2957, MARCH 1987

- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54ACT11030 . . . J PACKAGE
74ACT11030 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11030 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

description

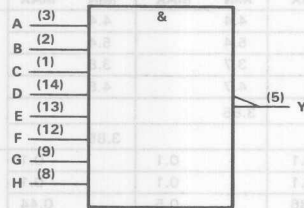
These devices contain a single 8-input NAND gate and perform the following Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \text{ OR}$$

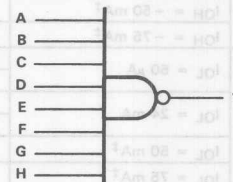
$$Y = \overline{A + B + C + D + E + F + G + H}$$

The 54ACT11030 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74ACT11030 is characterized for operation from -40°C to 85°C .

logic symbol†



logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J, D, and N packages.

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54ACT11030, 74ACT11030

8-INPUT POSITIVE-NAND GATES

TEST CONDITIONS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	-65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11030		74ACT11030		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		-24		-24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta V/\Delta t$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			54ACT11030		74ACT11030		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	$I_{OH} = -50 \text{ mA}^\ddagger$	5.5 V				3.85				
	$I_{OH} = -75 \text{ mA}^\ddagger$	5.5 V						3.85		
V_{OL}	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1	0.1		0.1		V
		5.5 V			0.1	0.1		0.1		
	$I_{OL} = 24 \text{ mA}$	4.5 V			0.36	0.5		0.44		
		5.5 V			0.36	0.5		0.44		
	$I_{OL} = 50 \text{ mA}^\ddagger$	5.5 V				1.65				
	$I_{OL} = 75 \text{ mA}^\ddagger$	5.5 V						1.65		
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1	±1		±1		μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4	80		40		μA
ΔI_{CC}	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9	1		1		mA
C_i	$V_I = V_{CC}$ or GND	5 V			3.5					pF

‡Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

2

Advanced CMOS Circuits

54ACT11030, 74ACT11030 8-INPUT POSITIVE-NAND GATES

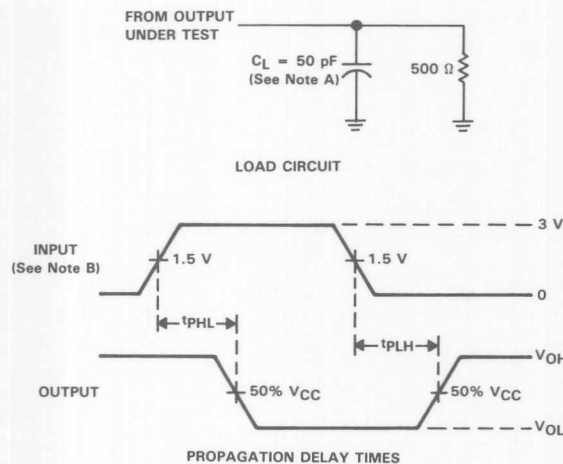
switching characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11030		74ACT11030		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	5.4	8.1	1.5	8.8	1.5	8.5	ns
t_{PHL}			1.5	5.9	7.8	1.5	9.3	1.5	8.7	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per gate	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	41	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

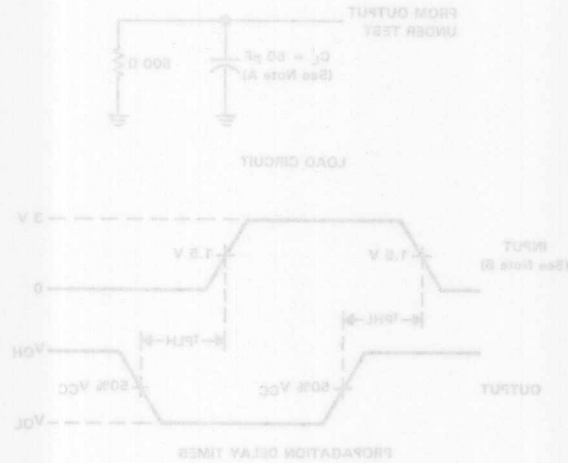
B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.

C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generator having the following characteristics: PRR ≤ 10 MHz, $t_r = 20$ ns, $V_H = 3.0$ V, $V_L = 0$ V.
C. The outputs are measured one at a time with one input transition per measurement.



PARAMETER MEASUREMENT INFORMATION

PARAMETER	TEST CONDITIONS	UNIT
C_{DD}	Power dissipation capacitance per gate $C_L = 50$ pF, $f = 1$ MHz	pF
	TYP	UNIT
	41	pF

operating characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$	74ACT11030	74ACT11030	UNIT
t_{PLH}	Y		MIN	MAX	MIN	MAX
t_{PLH}			1.5	8.4	8.1	8.8
t_{PLH}			1.5	8.8	8.3	8.7

switching characteristics, $V_{CC} = 5$ V ± 0.5 V (see Figure 1)

54AC11032, 74AC11032 QUADRUPLE 2-INPUT POSITIVE-OR GATES

D2957, JULY 1987—REVISED OCTOBER 1987

- New Flow-Through Architecture to Optimize PCB Layout

- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise

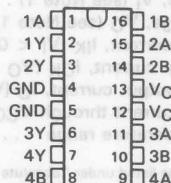
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process

- 500-mA Typical Latch-Up Immunity at 125°C

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

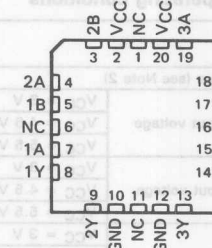
54AC11032 . . . J PACKAGE
74AC11032 . . . D OR N PACKAGE

(TOP VIEW)



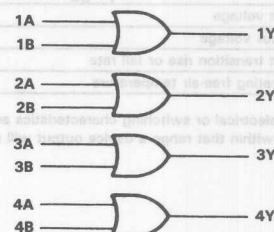
54AC11032 . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



description

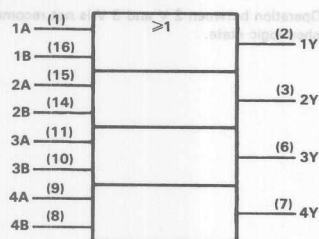
These devices contain four independent 2-input OR gates. They perform the Boolean functions $Y = A + B$ or $Y = \overline{A \cdot B}$ in positive logic.

The 54AC11032 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74AC11032 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

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54AC11032, 74AC11032 QUADRUPLE 2-INPUT POSITIVE-OR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC}+0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC}+0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Storage temperature range	-65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11032			74AC11032			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3$ V	2.1			2.1			V
		$V_{CC} = 4.5$ V	3.15			3.15			V
		$V_{CC} = 5.5$ V	3.85			3.85			V
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V			0.9			0.9	V
		$V_{CC} = 4.5$ V			1.35			1.35	V
		$V_{CC} = 5.5$ V			1.65			1.65	V
I_{OH}	High-level output current	$V_{CC} = 3$ V			-4			-4	mA
		$V_{CC} = 4.5$ V			-24			-24	mA
		$V_{CC} = 5.5$ V			-24			-24	mA
I_{OL}	Low-level output current	$V_{CC} = 3$ V			12			12	mA
		$V_{CC} = 4.5$ V			24			24	mA
		$V_{CC} = 5.5$ V			24			24	mA
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: No electrical or switching characteristics are specified at $V_{CC} < 3$ V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

2

Advanced CMOS Circuits

54AC11032, 74AC11032
QUADRUPL 2-INPUT POSITIVE-OR GATES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11032		74AC11032		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
V _{OL}	I _{OL} = 50 µA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	µA
	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		80		40	µA
C _I	V _I = V _{CC} or GND	5 V		3.5						pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C			54AC11032		74AC11032		UNIT		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t _{PLH}	A or B	Y	3.3 ± 0.3 V	1.5	6.3	8.7	1.5	10.7	1.5	9.7	ns		
			5 ± 0.5 V	1	4.3	6.2	1.5	7.3	1.5	6.7			
t _{PHL}			3.3 ± 0.3 V	1.5	5.4	7.4	1.5	8.5	1.5	8			
			5 ± 0.5 V	1	3.8	5.5	1.5	6.3	1.5	5.9			

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per gate	C _L = 50 pF, f = 1 MHz	24	pF

2 Advanced CMOS Circuits

Timing diagram for the 74VHC00 inverter. The diagram shows the input and output waveforms. The input signal transitions from 0V to 50% V_{CC} and back to 0V. The output signal transitions from V_{OH} to V_{OL} and back to V_{OH} . The propagation delay times are marked: t_{PLH} (low-to-high) and t_{PLH} (high-to-low). The load circuit consists of a 50 pF capacitor and a 500 ohm resistor connected to ground. The test conditions are specified as $V_{OH} = 5.0V$ and $V_{OL} = 0V$.

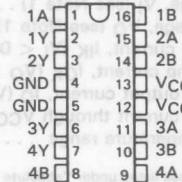
FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54ACT11032, 74ACT11032 QUADRUPLE 2-INPUT POSITIVE-OR GATES

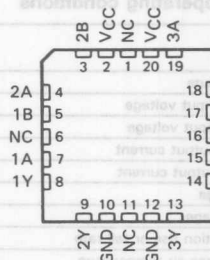
D2957, JULY 1987—REVISED OCTOBER 1987

- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54ACT11032 . . . J PACKAGE
74ACT11032 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11032 . . . FK PACKAGE
(TOP VIEW)



description

These devices contain four independent 2-input OR gates. They perform the Boolean functions $Y = A + B$ or $Y = \overline{A} \cdot \overline{B}$ positive logic.

The 54ACT11032 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11032 is characterized for operation from -40°C to 85°C.

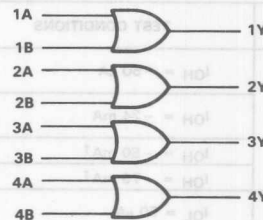
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

NC—No internal connection

logic diagram (positive logic)



FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

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TEXAS
INSTRUMENTS

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54ACT11032, 74ACT11032 QUADRUPLE 2-INPUT POSITIVE-OR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	–0.5 V to 7 V
Input voltage, V_I (see Note 1)	–0.5 V to $V_{CC}+0.5$ V
Output voltage, V_O (see Note 1)	–0.5 V to $V_{CC}+0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	–65°C to 150°C

[†]Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11032		74ACT11032		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		–24		–24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			54ACT11032		74ACT11032		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	$I_{OH} = -50 \text{ mA}^\dagger$	5.5 V				3.85				
V_{OL}	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	$I_{OL} = 24 \text{ mA}$	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	$I_{OL} = 50 \text{ mA}^\dagger$	5.5 V					1.65			
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		80		40	
ΔI_{CC}^\ddagger	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V			3.5					pF

[‡]Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[§]This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

2

Advanced CMOS Circuits

54ACT11032, 74ACT11032 QUADRUPL 2-INPUT POSITIVE-OR GATES

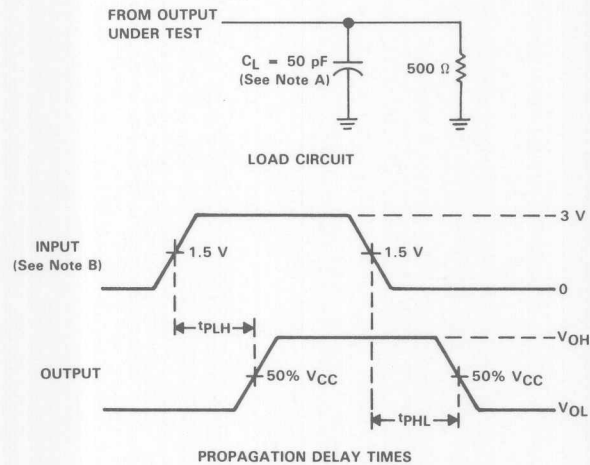
switching characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11032		74ACT11032		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	6.2	8.1	1.5	9.6	1.5	9	ns
t_{PHL}			1.5	4.9	7.4	1.5	8.4	1.5	8	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per gate	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	25	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\text{ }\Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.

C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

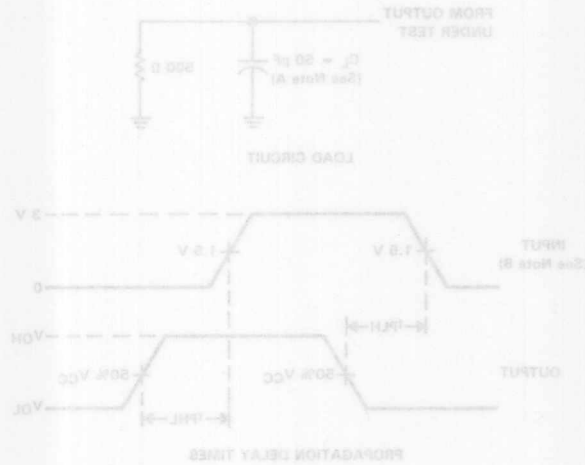
switching characteristics, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$				UNIT
			MIN	Typ	MAX	MIN	
t _{PLH}	A or B	Y	1.5	0.3	0.7	1.5	ns
			1.5	0.3	0.7	1.5	ns

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		UNIT
C _{pd} Power dissipation capacitance per gate		C _L = 50 pF, f = 1 MHz		
		Typ		20
		Limit		50

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Input signals are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, P = 2 mW, r_i = 2 Ω.
C. The outputs are measured one at a time with one input transition per measurement.

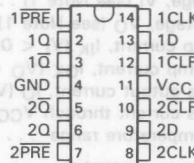
FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54AC11074, 74AC11074 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

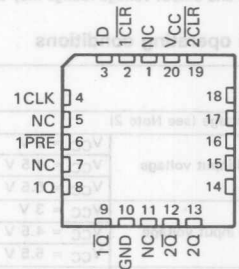
D2957, DECEMBER 1986—REVISED MARCH 1987

- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54AC11074 . . . J PACKAGE
74AC11074 . . . D OR N PACKAGE
(TOP VIEW)



54AC11074 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the Preset or Clear input sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the low-to-high transition of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

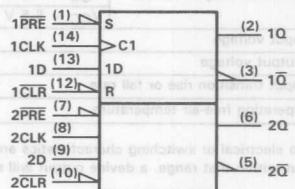
The 54AC11074 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC11074 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q-bar
L	H	X	X	H	L
H	L	X	X	H [†]	H [†]
L	L	X	X	H [†]	H [†]
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	Q ₀ -bar

[†] This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high level).

logic symbol[‡]



[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

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54AC11074, 74AC11074 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC}+0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC}+0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Storage temperature range	-65°C to 150°C

[†]Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54AC11074			74AC11074			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)	3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3$ V		2.1	$V_{CC} = 3$ V		2.1	V
		$V_{CC} = 4.5$ V		3.15	$V_{CC} = 4.5$ V		3.15	
		$V_{CC} = 5.5$ V		3.85	$V_{CC} = 5.5$ V		3.85	
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V		0.9	$V_{CC} = 3$ V		0.9	V
		$V_{CC} = 4.5$ V		1.35	$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 5.5$ V		1.65	$V_{CC} = 5.5$ V		1.65	
I_{OH}	High-level output current	$V_{CC} = 3$ V		-4	$V_{CC} = 3$ V		-4	mA
		$V_{CC} = 4.5$ V		-24	$V_{CC} = 4.5$ V		-24	
		$V_{CC} = 5.5$ V		-24	$V_{CC} = 5.5$ V		-24	
I_{OL}	Low-level output current	$V_{CC} = 3$ V		12	$V_{CC} = 3$ V		12	mA
		$V_{CC} = 4.5$ V		24	$V_{CC} = 4.5$ V		24	
		$V_{CC} = 5.5$ V		24	$V_{CC} = 5.5$ V		24	
V_I	Input voltage	0	V_{CC}		0	V_{CC}		V
V_O	Output voltage	0	V_{CC}		0	V_{CC}		V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10		0	10		ns/V
T_A	Operating free-air temperature	-55	125		-40	85		°C

NOTE 2: No electrical or switching characteristics are specified at $V_{CC} < 3$ V. Operation between 2 V and 3 V is not recommended, but within that range, a device output will maintain a previously established logic state.

INPUTS		PRESET		CLEAR		CLK		Q	
H	L	X	X	X	X	X	X	L	H
L	H	X	X	X	X	X	X	H	L
H	H	X	X	X	X	X	X	H	H
L	L	X	X	X	X	X	X	L	L
H	L	X	X	X	X	X	X	H	L
L	H	X	X	X	X	X	X	L	H
H	H	X	X	X	X	X	X	H	H
L	L	X	X	X	X	X	X	L	L

[†]This condition is nonreleasable; that is, it will not occur when either Preset or Clear returns to its inactive (high) level.

54AC11074, 74AC11074
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH CLEAR AND PRESET

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11074		74AC11074		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
	I _{OH} = -24 mA	5.5 V	4.94			4.7		4.8		
V _{OL}	I _{OH} = -50 mA [†]	5.5 V				3.85				V
	I _{OH} = -75 mA [†]	5.5 V						3.85		
	I _{OL} = 50 μA	3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	
I _I	V _I = V _{CC} or GND	4.5 V			0.36		0.5		0.44	μA
		5.5 V			0.36		0.5		0.44	
		5.5 V				1.65				
		5.5 V						1.65		
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		80		40	μA
C _i	V _I = V _{CC} or GND	5 V		3.5						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements (see Figure 1)

		V _{CC} RANGE	T _A = 25°C		54AC11074		74AC11074		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	3.3 ± 0.3 V	0	100	0	100	0	100	MHz
		5 ± 0.5 V	0	125	0	125	0	125	
t _w	Pulse duration	PRE or CLR low	3.3 ± 0.3 V	4	4	4	4	4	ns
			5 ± 0.5 V	4	4	4	4	4	
		CLK low or	3.3 ± 0.3 V	5	5	5	5	5	
		CLK high	5 ± 0.5 V	4	4	4	4	4	
t _{su}	Setup time data before CLK [†]	Data high or low	3.3 ± 0.3 V	5	5	5	5	5	ns
			5 ± 0.5 V	3.5	3.5	3.5	3.5	3.5	
		PRE or CLR inactive	3.3 ± 0.3 V	1	1	1	1	1	
			5 ± 0.5 V	1	1	1	1	1	
t _h	Hold time data after CLK [†]		3.3 ± 0.3 V	0	0	0	0	0	ns
			5 ± 0.5 V	0	0	0	0	0	

54AC11074, 74AC11074
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH CLEAR AND PRESET

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C			54AC11074		74AC11074		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			3.3 ± 0.3 V	100	125		100		100		MHz
			5 ± 0.5 V	125	150		125		125		
t _{PLH}	PRE or CLR	Q or \bar{Q}	3.3 ± 0.3 V	1.5	5.8	9.3	1.5	10.5	1.5	10	ns
			5 ± 0.5 V	1.5	4.2	6.6	1.5	7.5	1.5	7.1	
t _{PHL}	CLR	Q or \bar{Q}	3.3 ± 0.3 V	1.5	6.5	11.4	1.5	12.9	1.5	12.2	ns
			5 ± 0.5 V	1.5	4.7	8.2	1.5	9.6	1.5	9	
t _{PLH}	CLK	Q or \bar{Q}	3.3 ± 0.3 V	1.5	7.7	10.5	1.5	12.1	1.5	11.3	ns
			5 ± 0.5 V	1.5	5.4	7.5	1.5	8.7	1.5	8.2	
t _{PHL}	CLK	Q or \bar{Q}	3.3 ± 0.3 V	1.5	7.3	9.7	1.5	11.3	1.5	10.6	ns
			5 ± 0.5 V	1.5	5	6.9	1.5	8	1.5	7.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per flip-flop C _L = 50 pF, f = 1 MHz	30	pF

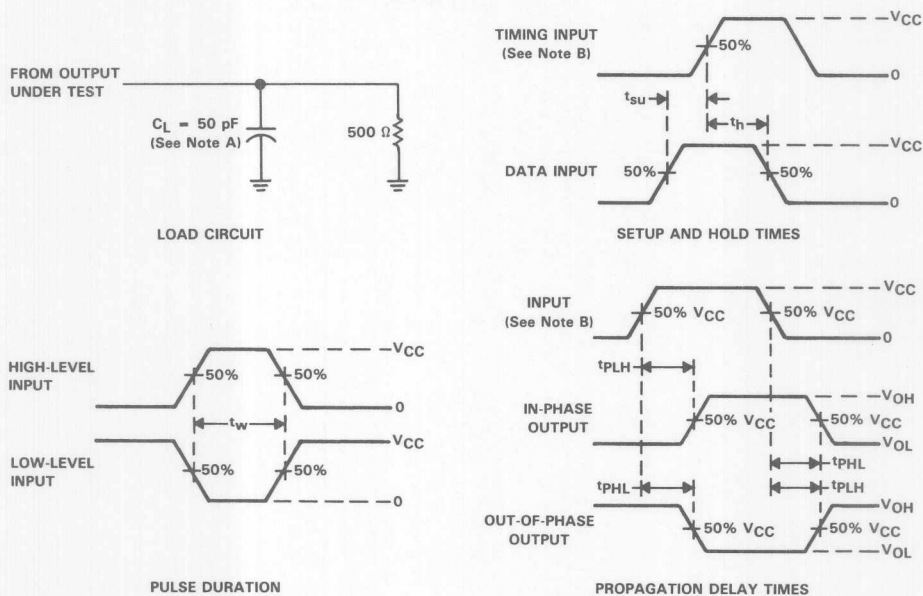
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Advanced CMOS Circuits

UNIT	74AC11074	54AC11074	T _A = 25°C	V _{CC}		Clock frequency	Pulse duration	Setup time data or low	Hold time data after CLK
				MIN	MAX				
MHz	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0
ns	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0
ns	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0
ns	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0
ns	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0

54AC11074, 74AC11074
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH CLEAR AND PRESET

PARAMETER MEASUREMENT INFORMATION

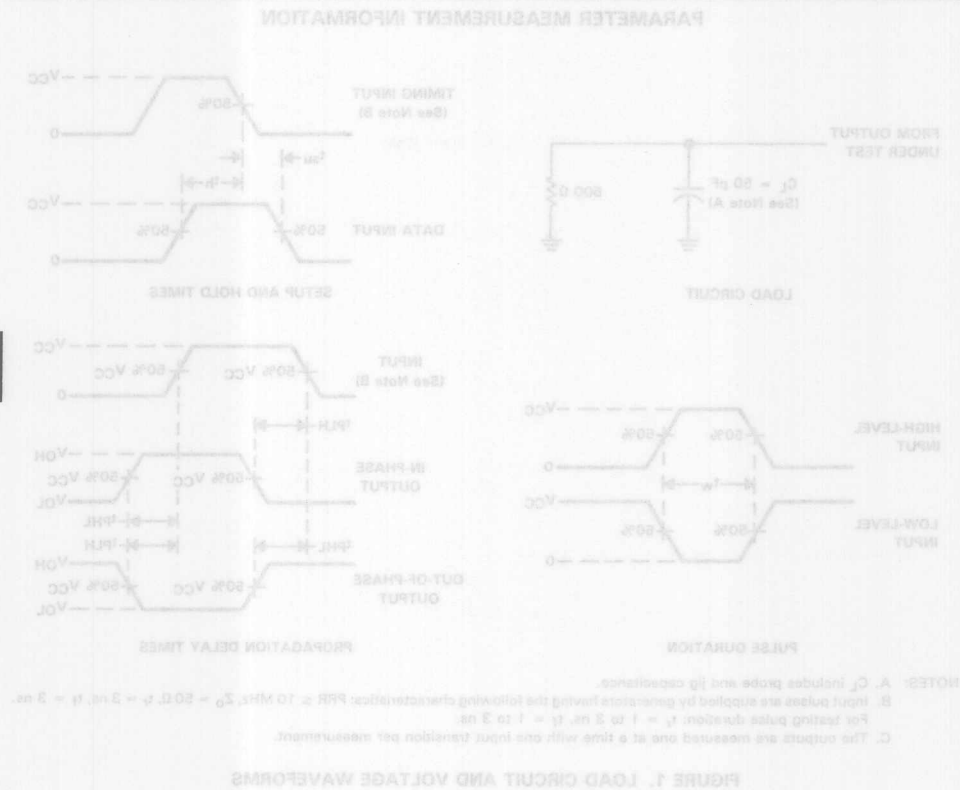


- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
For testing pulse duration: $t_r = 1 \text{ to } 3 \text{ ns}$, $t_f = 1 \text{ to } 3 \text{ ns}$.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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Advanced CMOS Circuits

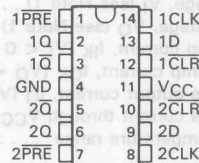


54ACT11074, 74ACT11074 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

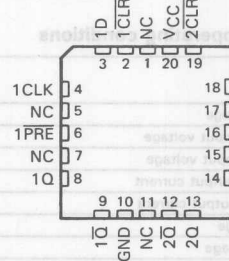
D2957, DECEMBER 1986—REVISED MARCH 1987

- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54ACT11074 . . . J PACKAGE
74ACT11074 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11074 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the Preset or Clear input sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the low-to-high transition of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

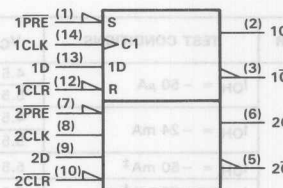
The 54ACT11074 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11074 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	Q̄ ₀

† This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high level).

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

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54ACT11074, 74ACT11074 **DUAL D-TYPE POSITIVE-EDGE-TRIGGERED** **FLIP-FLOPS WITH CLEAR AND PRESET**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to $V_{CC}+0.5$ V
Output voltage, V_O (see Note 1)	−0.5 V to $V_{CC}+0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	−65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11074		74ACT11074		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			54ACT11074		74ACT11074		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	$I_{OH} = -50 \text{ mA}^\ddagger$	5.5 V				3.85				
V_{OL}	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	$I_{OL} = 24 \text{ mA}$	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	$I_{OL} = 50 \text{ mA}^\ddagger$	5.5 V					1.65			
	$I_{OL} = 75 \text{ mA}^\ddagger$	5.5 V							1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		80		40	μA
ΔI_{CC}^\S	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V			3.5					pF

‡Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.

§This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

54ACT11074, 74ACT11074
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH CLEAR AND PRESET

timing requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see Figure 1)

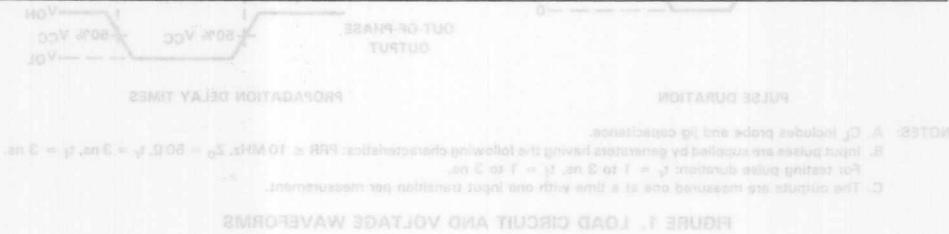
			$T_A = 25^\circ\text{C}$		54ACT11074		74ACT11074		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	100	0	100	MHz
t_w	Pulse duration	PRE or CLR low	5		5		5		ns
		CLK low or CLK high	5		5		5		
t_{su}	Setup time data before CLK†	Data high or low	4.5		4.5		4.5		ns
		PRE or CLR inactive	2		2		2		
t_h	Hold time data after CLK†		0		0		0		ns

switching characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11074		74ACT11074		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	125		100		100		MHz
t_{PLH}	PRE or CLR	Q or \bar{Q}	1.5	5.7	8.9	1.5	10.1	1.5	9.6	ns
t_{PHL}			1.5	6.6	11.3	1.5	13.3	1.5	12.5	
t_{PLH}	CLK	Q or \bar{Q}	1.5	6	8.5	1.5	10	1.5	9.4	ns
t_{PHL}			1.5	5.7	8	1.5	9.4	1.5	8.8	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	$C_L = 50\text{ pF}$,	$f = 1\text{ MHz}$	30	pF



NOTES: A. CL includes probe and jig capacitance.
 B. Input buffers are enabled by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $t_r = 80\text{ pF}$, $t_f = 3\text{ ns}$.
 C. The outputs are measured one at a time with one input transition per measurement.
 D. For testing pulse duration $t = 1$ to 3 ns and $t = 1$ to 3 ns .

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

2

Advanced CMOS Circuits

54ACT11074, 74ACT11074
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH CLEAR AND PRESET

PARAMETER MEASUREMENT INFORMATION

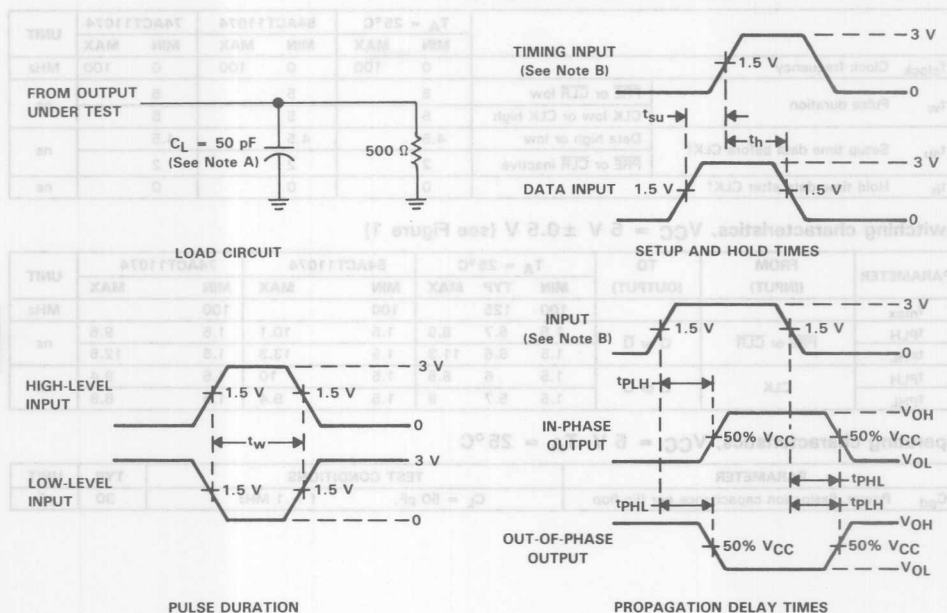


FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

2

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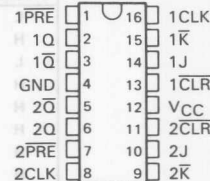
54AC11109, 74AC11109 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

D2957, MARCH 1987

- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125 °C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

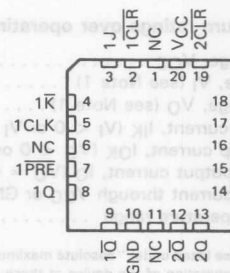
54AC11109 ... J PACKAGE
74AC11109 ... D OR N PACKAGE

(TOP VIEW)



54AC11109 ... FK PACKAGE

(TOP VIEW)



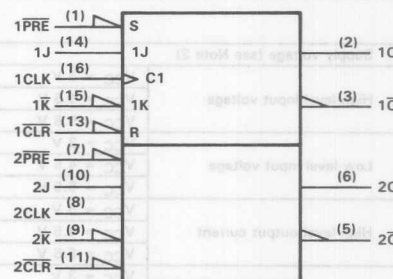
NC—No internal connection

description

These devices contain two independent J-K positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding K and tying J high. They also can perform as D-type flip-flops by tying the J and K inputs together.

The 54AC11109 is characterized for operation over the full military temperature range of -55 °C to 125 °C. The 74AC11109 is characterized for operation from -40 °C to 85 °C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

2

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54AC11109, 74AC11109 **DUAL J-K POSITIVE-EDGE-TRIGGERED** **FLIP-FLOPS WITH CLEAR AND PRESET**

FUNCTION TABLE (each gate)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	\bar{K}	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H [†]	H [†]
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q ₀	\bar{Q}_0
H	H	↑	H	H	H	L
H	H	L	X	X	Q ₀	\bar{Q}_0

[†] This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to the inactive (high) level.

2

Advanced CMOS Circuits

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to $V_{CC}+0.5$ V
Output voltage, V_O (see Note 1)	−0.5 V to $V_{CC}+0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	−65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54AC11109			74AC11109			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)	3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3$ V		2.1	2.1			V
		$V_{CC} = 4.5$ V		3.15	3.15			
		$V_{CC} = 5.5$ V		3.85	3.85			
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V			0.9		0.9	V
		$V_{CC} = 4.5$ V			1.35		1.35	
		$V_{CC} = 5.5$ V			1.65		1.65	
I_{OH}	High-level output current	$V_{CC} = 3$ V			−4		−4	mA
		$V_{CC} = 4.5$ V			−24		−24	
		$V_{CC} = 5.5$ V			−24		−24	
I_{OL}	Low-level output current	$V_{CC} = 3$ V			12		12	mA
		$V_{CC} = 4.5$ V			24		24	
		$V_{CC} = 5.5$ V			24		24	
V_I	Input voltage	0	V_{CC}		0	V_{CC}		V
V_O	Output voltage	0	V_{CC}		0	V_{CC}		V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	0	10		ns/V
T_A	Operating free-air temperature	−55	125		−40	85		°C

NOTE 2: No electrical or switching characteristics are specified at $V_{CC} < 3$ V. Operation between 2 V and 3 V is not recommended, but within that range, a device output will maintain a previously established logic state.

54AC11109, 74AC11109
DUAL J-K POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH CLEAR AND PRESET

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11109		74AC11109		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
	I _{OH} = -24 mA	5.5 V	4.94			4.7		4.8		
V _{OL}	I _{OL} = 50 µA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
	I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	
I _I	I _{OL} = 50 mA [†]	5.5 V				1.65				µA
		5.5 V						1.65		
		5.5 V								
	I _{OL} = 75 mA [†]	5.5 V								
		5.5 V								
		5.5 V								
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		80		40	µA
C _i	V _I = V _{CC} or GND	5 V		3.5						pF

[†]Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements (see Figure 1)

PARAMETER		V _{CC} RANGE	T _A = 25°C		54AC11109		74AC11109		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	3.3 ± 0.3 V	0	70	0	70	0	70	MHz
		5 ± 0.5 V	0	100	0	100	0	100	
t _w	Pulse duration	PRE or CLR low	3.3 ± 0.3 V	5	5	5	5	5	ns
		CLK high or low	3.3 ± 0.3 V	7.2	7.2	7.2	7.2	7.2	
	Setup time before CLK †	PRE or CLR inactive	5 ± 0.5 V	4	5	4	5	4	
		CLK high or low	5 ± 0.5 V	5	5	5	5	5	
t _{su}	Data high or low	3.3 ± 0.3 V	5.5	5.5	5.5	5.5	5.5	5.5	ns
		5 ± 0.5 V	4.5	4.5	4.5	4.5	4.5	4.5	
	PRE or CLR inactive	3.3 ± 0.3 V	2.5	2.5	2.5	2.5	2.5	2.5	
		5 ± 0.5 V	2	2	2	2	2	2	
t _h	Hold time, data after CLK †	3.3 ± 0.3 V	0	0	0	0	0	0	ns
		5 ± 0.5 V	0	0	0	0	0	0	

54AC11109, 74AC11109
DUAL J-K POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH CLEAR AND PRESET

switching characteristics over recommended operating free-air temperature range (see Figure 1)

PARAMETER	FROM	TO	V _{CC} RANGE	T _A = 25°C			54AC11109		74AC11109		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			3.3 ± 0.3 V	70	100		70		70		MHz
			5 ± 0.5 V	100	125		100		100		
t _{PLH}	PRE or CLR	Q or \bar{Q}	3.3 ± 0.3 V	1.5	6.5	9	1.5	10.5	1.5	9.9	ns
			5 ± 0.5 V	1.5	4.5	6.5	1.5	7.6	1.5	7.1	
t _{PHL}			3.3 ± 0.3 V	1.5	8	12.6	1.5	14.4	1.5	13.7	
			5 ± 0.5 V	1.5	5	8.6	1.5	10.2	1.5	9.6	
t _{PLH}	CLK	Q or \bar{Q}	3.3 ± 0.3 V	1.5	8	11.4	1.5	13.5	1.5	12.7	ns
			5 ± 0.5 V	1.5	5.5	7.9	1.5	9.4	1.5	8.8	
t _{PHL}			3.3 ± 0.3 V	1.5	7.5	10.5	1.5	12.7	1.5	11.8	
			5 ± 0.5 V	1.5	5	7.3	1.5	8.6	1.5	8.1	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per flip-flop C _L = 50 pF, f = 1 MHz	32	pF

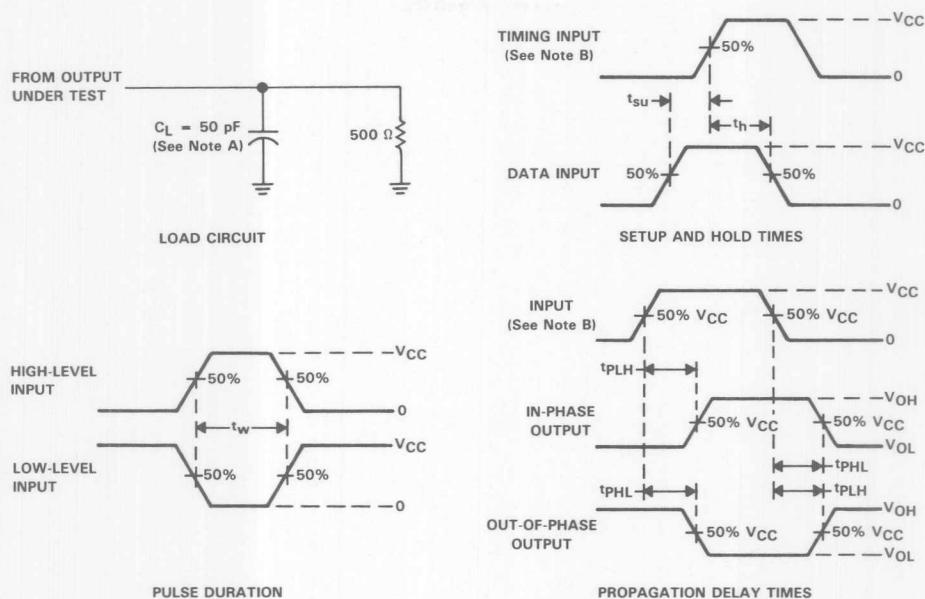
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Advanced CMOS Circuits

UNIT	PARAMETER		V _{CC} RANGE		T _A = 25°C		54AC11109		74AC11109	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
MHz	Clock frequency	f _{CLK}	3.3 ± 0.3 V	0	0	0	0	0	0	0
			5 ± 0.5 V	0	0	0	0	0	0	0
	Pulse duration	t _P	3.3 ± 0.3 V	8	8	8	8	8	8	8
			5 ± 0.5 V	8	8	8	8	8	8	8
ns	Setup time	t _S	3.3 ± 0.3 V	4.5	4.5	4.5	4.5	4.5	4.5	4.5
			5 ± 0.5 V	4.5	4.5	4.5	4.5	4.5	4.5	4.5
	Hold time	t _H	3.3 ± 0.3 V	0	0	0	0	0	0	0
			5 ± 0.5 V	0	0	0	0	0	0	0

54AC11109, 74AC11109
DUAL J-K POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH CLEAR AND PRESET

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 For testing pulse duration: $t_r = 1 \text{ to } 3 \text{ ns}$, $t_f = 1 \text{ to } 3 \text{ ns}$.
 C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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Advanced CMOS Circuits

PARAMETER MEASUREMENT INFORMATION

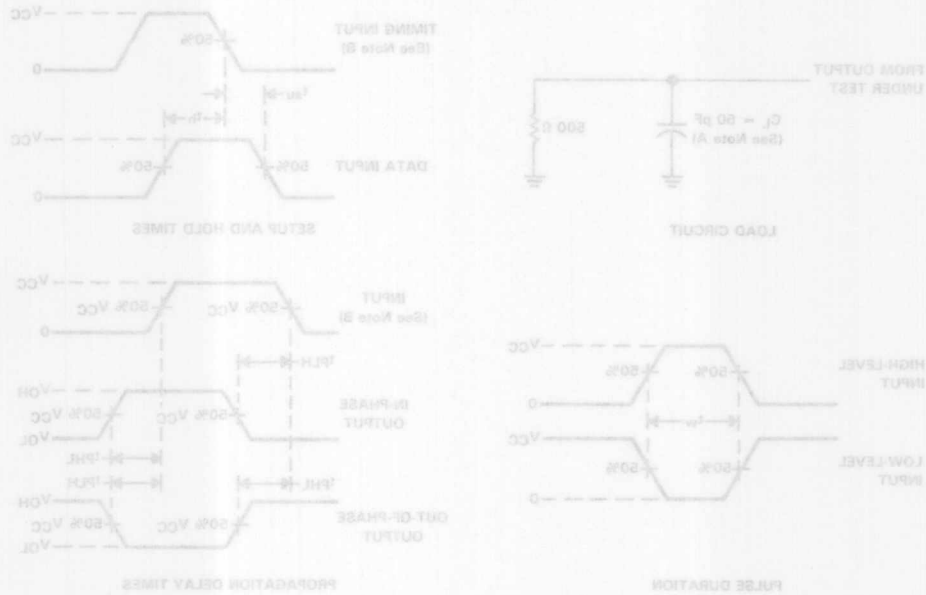


FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

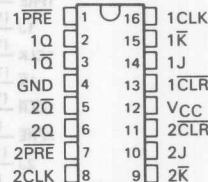
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generator having the following characteristics: PRR = 10 MHz, $V_p = 50$ V, $V_r = 3$ V.
C. The outputs are measured one at a time with one input transition per measurement.

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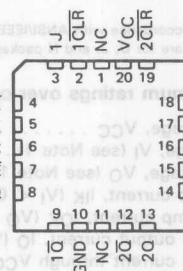
54ACT11109, 74ACT11109
DUAL J-K POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH CLEAR AND PRESET
D2957, FEBRUARY 1987—REVISED MARCH 1987

- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54ACT11109 ... J PACKAGE
74ACT11109 ... D OR N PACKAGE
(TOP VIEW)



54ACT11109 ... FK PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	\bar{K}	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H [†]	H [†]
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q ₀	\bar{Q}_0
H	H	↑	H	H	H	L
H	H	L	X	X	Q ₀	\bar{Q}_0

[†] This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to the inactive (high) level.

description

These devices contain two independent J-K positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and \bar{K} input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and \bar{K} inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding \bar{K} and tying J high. They also can perform as D-type flip-flops if J and \bar{K} are tied together.

The 54ACT11109 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11109 is characterized for operation from -40°C to 85°C.

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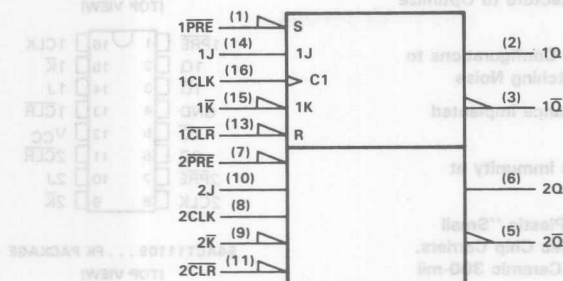
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INSTRUMENTS

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54ACT11109, 74ACT11109 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

	54ACT11109			74ACT11109			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			−24			−24	mA
I_{OL} Low-level output current			24			24	mA
V_I Input voltage	0		V_{CC}	0		V_{CC}	V
V_O Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$ Input transition rise or fall rate	0		10	0		10	ns/V
T_A Operating free-air temperature	−55		125	−40		85	°C

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Advanced CMOS Circuits

54ACT11109, 74ACT11109
DUAL J-K POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH CLEAR AND PRESET

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11109		74ACT11109		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
V _{OL}	I _{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA [†]	5.5 V				1.65				
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	µA
		5.5 V			4		80		40	
	I _{CC}	5.5 V			4		80		40	
		5.5 V			0.9		1		1	
	ΔI _{CC} [‡]	5.5 V			0.9		1		1	
C _I	V _I = V _{CC} or GND	5 V			3.5					pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements, V_{CC} = 5 ± 0.5 V (see Figure 1)

			T _A = 25°C			54ACT11109		74ACT11109		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		0	100		0	100	0	100	MHz
t _w	Pulse duration	PRE or CLR low	5.5			5.5		5.5		ns
		CLK high or low	5			5		5		
t _{su}	Setup time before CLK [†]	Data high or low	5.5			5.5		5.5		ns
		PRE or CLR inactive	2			2		2		
t _h	Hold time data after CLK [†]		0			0		0		ns

switching characteristics V_{CC} = 5 ± 0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54ACT11109		74ACT11109		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			100	125		100		100		MHz
t _{PLH}	PRE or CLR	Q or \bar{Q}	1.5	5.5	8.6	1.5	9.8	1.5	9.2	ns
t _{PHL}			1.5	6	10.8	1.5	12.6	1.5	11.8	
t _{PLH}	CLK	Q or \bar{Q}	1.5	6	8.3	1.5	9.7	1.5	9.1	ns
t _{PHL}			1.5	5.5	7.6	1.5	9	1.5	8.3	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per flip-flop C _L = 50 pF, f = 1 MHz	31	pF

54ACT11109, 74ACT11109
DUAL J-K POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH CLEAR AND PRESET

PARAMETER MEASUREMENT INFORMATION

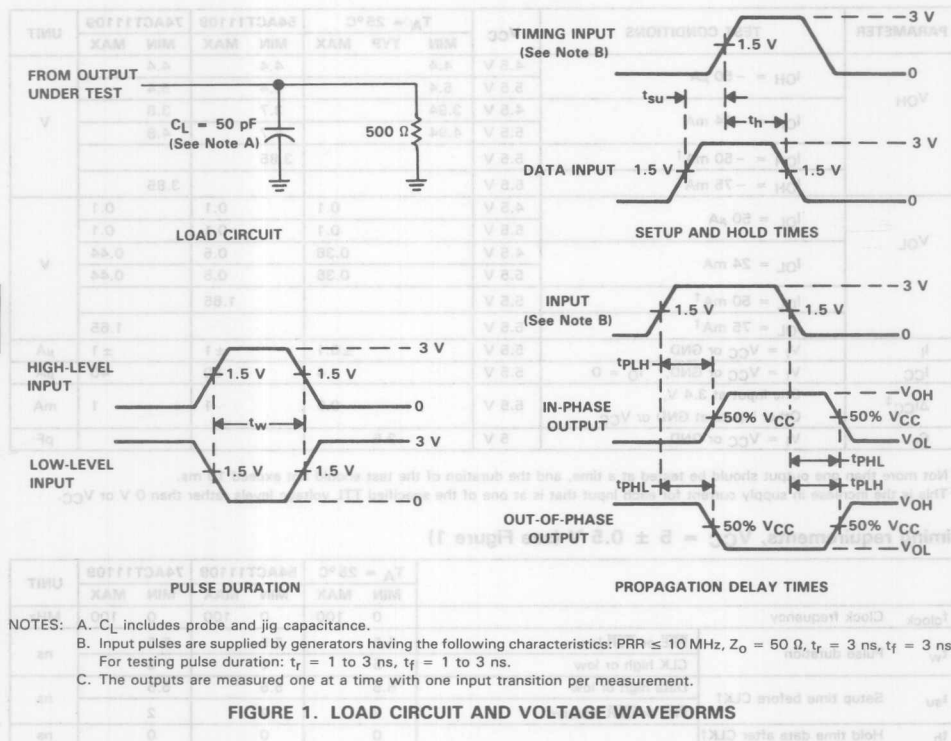


FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TA = 25°C	UNIT
t _{max}			100	ns
t _{PLH}			1.2	ns
t _{PLH}			1.2	ns
t _{PLH}			1.2	ns
t _{PLH}			1.2	ns
t _{PLH}			1.2	ns
t _{PLH}			1.2	ns
t _{PLH}			1.2	ns
t _{PLH}			1.2	ns
t _{PLH}			1.2	ns

PARAMETER	TEST CONDITIONS	UNIT
C _{int} Power dissipation capacitance per flip-flop	C _L = 50 pF, f = 1 MHz	pF
		27

2

Advanced CMOS Circuits

54AC11240, 74AC11240 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2957, MAY 1987

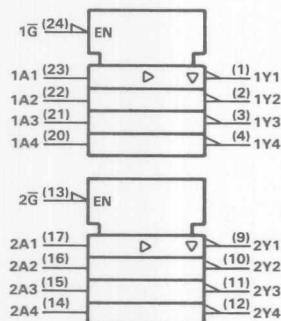
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices provide inverting outputs and symmetrical \bar{G} (active-low output control) inputs. These devices feature high fan-out and improved fan-in.

The 54AC11240 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC11240 is characterized for operation from -40°C to 85°C.

logic symbol†

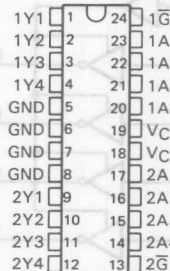


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

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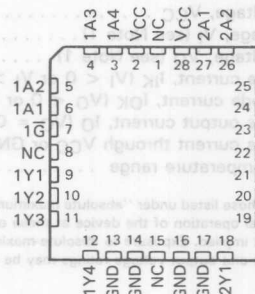
54AC11240 ... JT PACKAGE
74AC11240 ... DW OR NT PACKAGE

(TOP VIEW)



54AC11240 ... FK PACKAGE

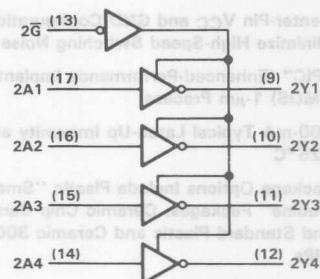
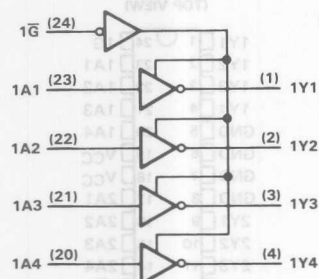
(TOP VIEW)



NC—No internal connection

54AC11240, 74AC11240 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

logic diagram (positive logic)



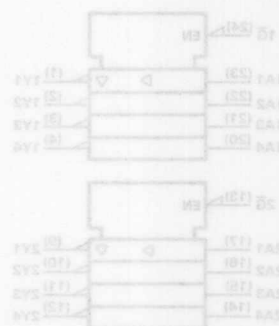
Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input diode current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output diode current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

[†]Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and EIA Publication B13-12.
Pin numbers shown are for DW, JT, and NT packages.

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54AC11240, 74AC11240
OCTAL BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	TEST CONDITIONS	UNIT	54AC11240			74AC11240		
			MIN	NOM	MAX	MIN	NOM	MAX
V _{CC}	Supply voltage (see Note 2)	V	3	5	5.5	3	5	5.5
V _{IH}	High-level input voltage	V	V _{CC} = 3 V			2.1		
			V _{CC} = 4.5 V			3.15		
			V _{CC} = 5.5 V			3.85		
V _{IL}	Low-level input voltage	V	V _{CC} = 3 V			0.9		
			V _{CC} = 4.5 V			1.35		
			V _{CC} = 5.5 V			1.65		
I _{OH}	High-level output current	mA	V _{CC} = 3 V			-4		
			V _{CC} = 4.5 V			-24		
			V _{CC} = 5.5 V			-24		
I _{OL}	Low-level output current	mA	V _{CC} = 3 V			12		
			V _{CC} = 4.5 V			24		
			V _{CC} = 5.5 V			24		
V _I	Input voltage	V	0		V _{CC}	0		V _{CC}
V _O	Output voltage	V	0		V _{CC}	0		V _{CC}
Δt/Δv	Input transition rise or fall rate	ns/V	G			5		
			Data			10		
T _A	Operating free-air temperature	°C	-55			125		

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range, a device output will maintain a previously established logic state.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C		T _A = 55°C		UNIT
				MIN	TYP	MIN	MAX	
t _{PLH}	A	Y	3.3 ± 0.3 V	1.2	7.5	1.0	13.0	ns
			2.7 ± 0.3 V	1.2	8.4	1.0	13.0	
			2.3 ± 0.3 V	1.0	8.3	1.0	13.0	
t _{PLL}	A	Y	3.3 ± 0.3 V	1.2	4.8	1.0	7.8	ns
			2.7 ± 0.3 V	1.2	4.8	1.0	7.8	
			2.3 ± 0.3 V	1.2	4.8	1.0	7.8	
t _{PSH}	G	Y	3.3 ± 0.3 V	1.2	8.3	1.0	13.0	ns
			2.7 ± 0.3 V	1.2	8.3	1.0	13.0	
			2.3 ± 0.3 V	1.2	8.3	1.0	13.0	
t _{PSL}	G	Y	3.3 ± 0.3 V	1.2	7.5	1.0	13.0	ns
			2.7 ± 0.3 V	1.2	8.3	1.0	13.0	
			2.3 ± 0.3 V	1.2	8.3	1.0	13.0	
t _{PHZ}	G	Y	3.3 ± 0.3 V	1.2	8.3	1.0	13.0	ns
			2.7 ± 0.3 V	1.2	8.3	1.0	13.0	
			2.3 ± 0.3 V	1.2	8.3	1.0	13.0	
t _{PLZ}	G	Y	3.3 ± 0.3 V	1.2	8.3	1.0	13.0	ns
			2.7 ± 0.3 V	1.2	8.3	1.0	13.0	
			2.3 ± 0.3 V	1.2	8.3	1.0	13.0	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	UNIT
C _{pd} Power dissipation capacitance per buffer	Outputs enabled	ps
	Outputs disabled	ps

54AC11240, 74AC11240 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11240		74AC11240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
I _{OH}	I _{OH} = -50 mA [†]	5.5 V				3.85				mA
	I _{OH} = -75 mA [†]	5.5 V						3.85		
V _{OL}	I _{OL} = 50 μA	3 V		0.1		0.1		0.1		V
		4.5 V		0.1		0.1		0.1		
		5.5 V		0.1		0.1		0.1		
	I _{OL} = 12 mA	3 V		0.36		0.5		0.44		
		4.5 V		0.36		0.5		0.44		
		5.5 V		0.36		0.5		0.44		
I _{OL}	I _{OL} = 50 mA [†]	5.5 V				1.65				mA
	I _{OL} = 75 mA [†]	5.5 V						1.65		
I _{OZ}	V _O = V _{CC} or GND	5.5 V		±0.5		±10		±5		μA
I _I	V _I = V _{CC} or GND	5.5 V		±0.1		±1		±1		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		8		160		80		μA
C _i	V _I = V _{CC} or GND	5 V		4						pF
C _o	V _O = V _{CC} or GND	5 V		10						pF

[†]Not more than one output should be tested at one time, and the duration of the test should not exceed 10 ms.

switching characteristics (see Figure 1)

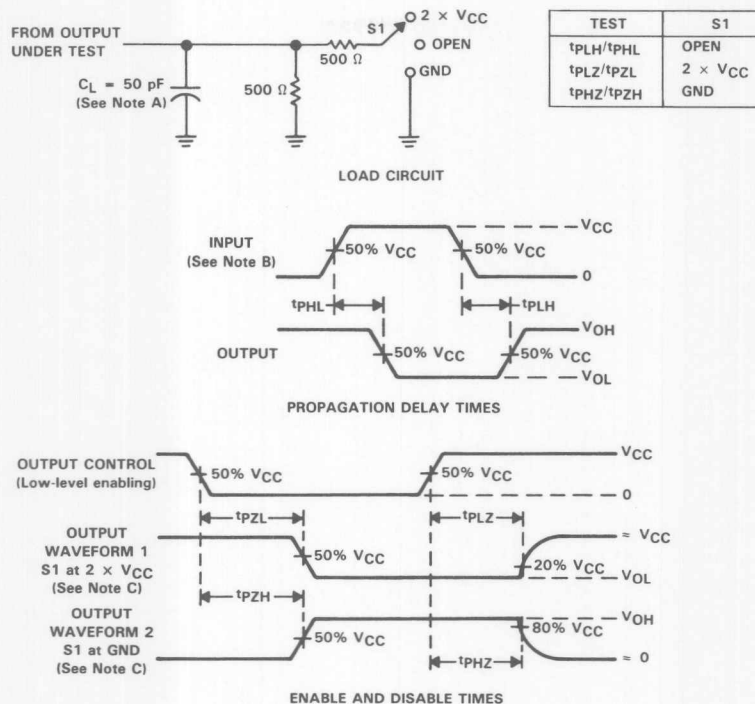
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C			54AC11240		74AC11240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	3.3 ± 0.3 V	1.5	7.6	10.5	1.5	12.8	1.5	11.7	ns
			5 ± 0.5 V	1.5	5.4	7.5	1.5	9	1.5	8.4	
t _{PHL}	A	Y	3.3 ± 0.3 V	1.5	6.3	8.6	1.5	10.2	1.5	9.5	ns
			5 ± 0.5 V	1.5	4.6	6.6	1.5	7.8	1.5	7.2	
t _{PZH}	\bar{A}	Y	3.3 ± 0.3 V	1.5	8.2	11.6	1.5	13.4	1.5	12.7	ns
			5 ± 0.5 V	1.5	5.7	8.2	1.5	9.9	1.5	9.2	
t _{PZL}	\bar{A}	Y	3.3 ± 0.3 V	1.5	7.6	10.8	1.5	13	1.5	12	ns
			5 ± 0.5 V	1.5	5.3	7.7	1.5	9.4	1.5	8.7	
t _{PHZ}	\bar{A}	Y	3.3 ± 0.3 V	1.5	5.5	7.5	1.5	8.1	1.5	7.8	ns
			5 ± 0.5 V	1.5	4.7	6.3	1.5	6.9	1.5	6.6	
t _{PLZ}	\bar{A}	Y	3.3 ± 0.3 V	1.5	6.7	9.4	1.5	10	1.5	9.8	ns
			5 ± 0.5 V	1.5	5.2	7.3	1.5	8	1.5	7.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per buffer	Outputs enabled	C _L = 50 pF, f = 1 MHz	39	pF
		Outputs disabled		12	

54AC11240, 74AC11240
OCTAL BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION

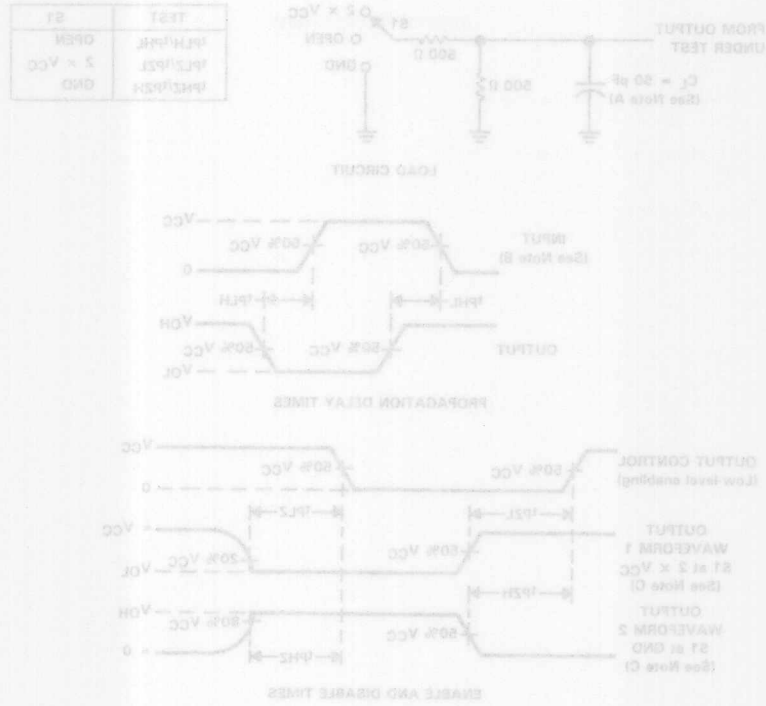


FIGURE 7. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input values are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $V_{OH} = 5.0 \text{ V}$, $V_{OL} = 0 \text{ V}$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

54ACT11240, 74ACT11240 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2957, MAY 1987

- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

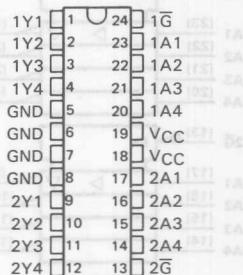
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices provide inverting outputs and symmetrical \bar{G} (active-low output control) inputs. These devices feature high fan-out and improved fan-in.

The 54ACT11240 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11240 is characterized for operation from -40°C to 85°C.

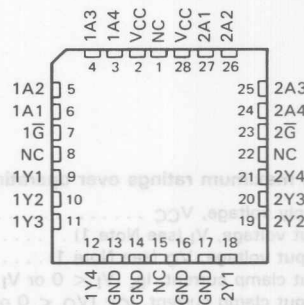
54ACT11240 . . . JT PACKAGE
74ACT11240 . . . DW OR NT PACKAGE

(TOP VIEW)



54ACT11240 . . . FK PACKAGE

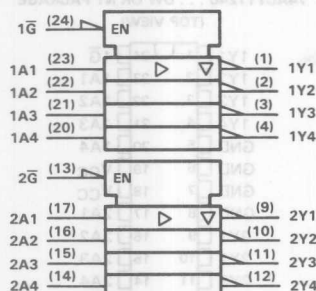
(TOP VIEW)



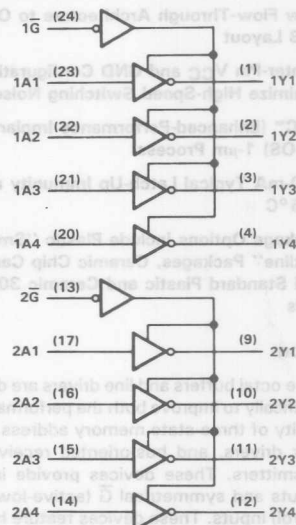
54ACT11240, 74ACT11240

OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

logic symbol†



logic diagram (positive logic)



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Advanced CMOS Circuits

†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±200 mA
Storage temperature range	−65°C to 150°C

‡Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

	54ACT11240			74ACT11240			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			−24			−24	mA
I_{OL} Low-level output current			24			24	mA
V_I Input voltage	0		V_{CC}	0		V_{CC}	V
V_O Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta V/\Delta t$ Input transition rise or fall rate	0		10	0		10	ns/V
T_A Operating free-air temperature	−55		125	−40		85	°C

54ACT11240, 74ACT11240 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11240		74ACT11240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
V _{OL}	I _{OH} = -75 mA [†]	5.5 V						3.85		V
	I _{OL} = 50 µA	4.5 V			0.1	0.1		0.1		
		5.5 V			0.1	0.1		0.1		
	I _{OL} = 24 mA	4.5 V			0.36	0.5		0.44		
		5.5 V			0.36	0.5		0.44		
	I _{OL} = 50 mA [†]	5.5 V				1.65				
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5	±10		±5		µA
	I _I = V _{CC} or GND	5.5 V			±0.1	±1		±1		
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8	160		80		µA
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.9	1		1		mA
C _i	V _I = V _{CC} or GND	5 V		4						pF
C _O	V _O = V _{CC} or GND	5 V		10						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics, V_{CC} = 5 V ± 0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54ACT11240		74ACT11240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	1.5	6.5	9.9	1.5	11.1	1.5	10.6	ns
t _{PHL}			1.5	6	8	1.5	9.2	1.5	8.7	
t _{PZH}	\bar{G}	Y	1.5	7.5	11.7	1.5	13.1	1.5	12.5	ns
t _{PZL}			1.5	7.3	11.5	1.5	12.8	1.5	12.3	
t _{PHZ}	\bar{G}	Y	1.5	7.3	9.4	1.5	10.3	1.5	10	ns
t _{PLZ}			1.5	7.9	10.3	1.5	11.2	1.5	10.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per buffer	Outputs enabled	C _L = 50 pF, f = 1 MHz	47	pF
		Outputs disabled		13	

2

Advanced CMOS Circuits

54ACT11240, 74ACT11240 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION

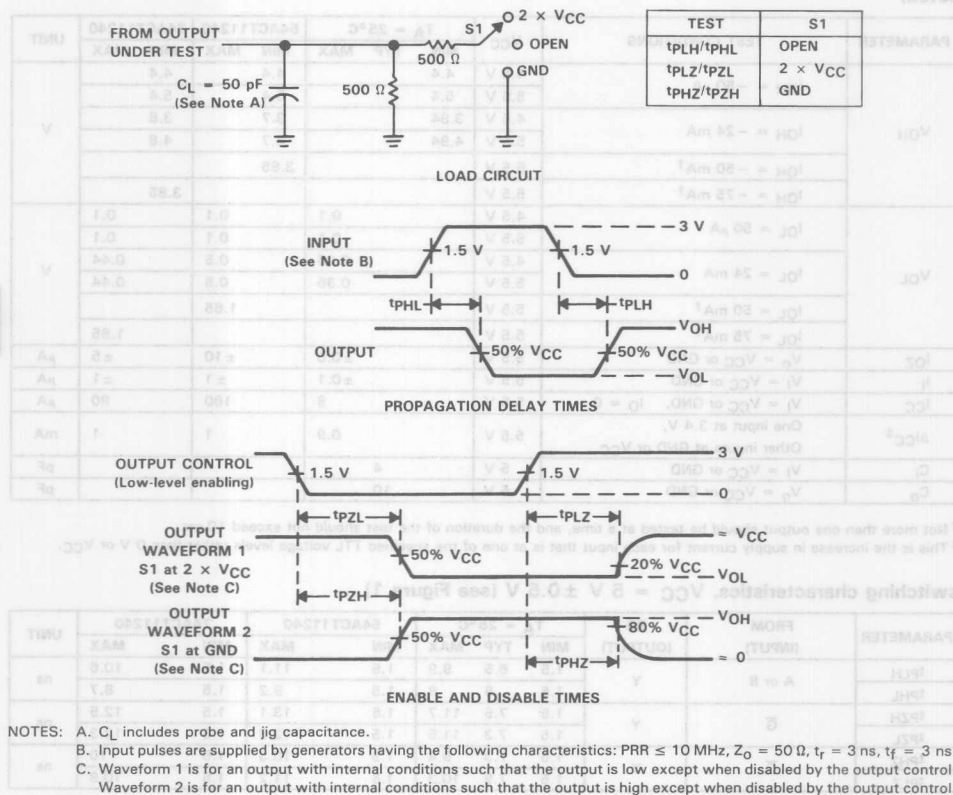


FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

PARAMETER	TEST CONDITIONS	UNIT
t_{PLH}	Output enabled	ns
t_{PLZ}	Output disabled	ns
t_{PHZ}	Output disabled	ns

54AC11241, 74AC11241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2957, JULY 1987

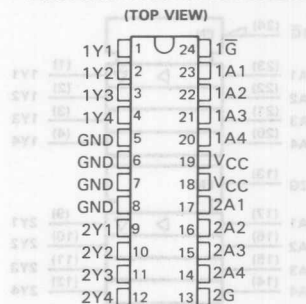
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

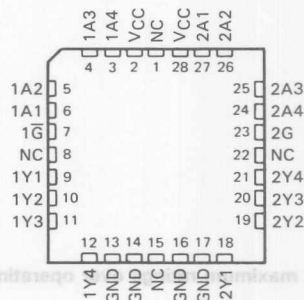
This octal buffer and line driver is designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. This device features a high fan-out.

The 54AC11241 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74AC11241 is characterized for operation from -40°C to 85°C .

54AC11241 ... JT PACKAGE
74AC11241 ... DW OR NT PACKAGE



54AC11241 ... FK PACKAGE
(TOP VIEW)



NC—No internal connection

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Advanced CMOS Circuits

PRODUCT PREVIEW

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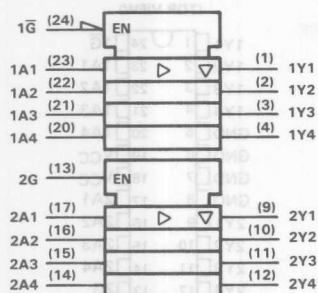


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D-113

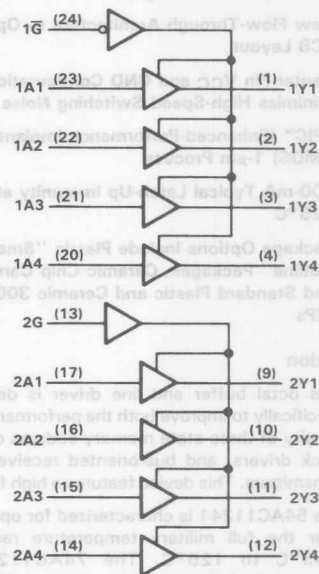
54AC11241, 74AC11241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers are for DW, JT, and NT packages.

2

Advanced CMOS Circuits

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54AC11241, 74AC11241
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

			54AC11241			74AC11241			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1			2.1			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 5.5 V	3.85			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V			0.9			9.9	V
		V _{CC} = 4.5 V			1.35			1.35	
		V _{CC} = 5.5 V			1.65			1.65	
I _{OH}	High-level output current	V _{CC} = 3 V			-4			-4	mA
		V _{CC} = 4.5 V			-24			-24	
		V _{CC} = 5.5 V			-24			-24	
I _{OL}	Low-level output current	V _{CC} = 3 V			12			12	mA
		V _{CC} = 4.5 V			24			24	
		V _{CC} = 5.5 V			24			24	
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise or fall rate		0		10	0		10	ns/V
T _A	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11241		74AC11241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
	I _{OH} = -24 mA	5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
	I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA [†]	5.5 V				1.65				
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±10		±5	μA
		5.5 V			±0.1		±1		±1	
		5.5 V			8		160		80	
	V _I = V _{CC} or GND	5 V			4					
		5 V			10					
	V _O = V _{CC} or GND	5 V								
		5 V								

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

54AC11241, 74AC11241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

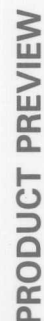
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C			54AC11241		74AC11241		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	3.3 ± 0.3 V								ns
			5 ± 0.5 V		7.5						
			3.3 ± 0.3 V								
t _{PHL}	A	Y	5 ± 0.5 V		6						ns
			3.3 ± 0.3 V								
			5 ± 0.5 V								
t _{PZH}	1G	Y	3.3 ± 0.3 V		7						ns
			5 ± 0.5 V								
			3.3 ± 0.3 V								
t _{PZL}	1G	Y	5 ± 0.5 V		6.6						ns
			3.3 ± 0.3 V								
			5 ± 0.5 V								
t _{PHZ}	1G	Y	3.3 ± 0.3 V		5.7						ns
			5 ± 0.5 V								
			3.3 ± 0.3 V								
t _{PLZ}	2G	Y	5 ± 0.5 V		6.5						ns
			3.3 ± 0.3 V								
			5 ± 0.5 V								
t _{PZH}	2G	Y	5 ± 0.5 V		5.8						ns
			3.3 ± 0.3 V								
			5 ± 0.5 V								
t _{PHZ}	2G	Y	3.3 ± 0.3 V		6.1						ns
			5 ± 0.5 V								
			3.3 ± 0.3 V								
t _{PLZ}	2G	Y	5 ± 0.5 V		6.8						ns
			3.3 ± 0.3 V								
			5 ± 0.5 V								

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per buffer	Outputs enabled	C _L = 50 pF, f = 1 MHz		26	pF
		Outputs disabled			10	
V	V _{OL}	0.1	0.1	0.1	0.1	10V
		0.2	0.2	0.2	0.2	
		0.3	0.3	0.3	0.3	
		0.4	0.4	0.4	0.4	
		0.5	0.5	0.5	0.5	
		0.6	0.6	0.6	0.6	
V	V _{OH}	0.1	0.1	0.1	0.1	10V
		0.2	0.2	0.2	0.2	
		0.3	0.3	0.3	0.3	
		0.4	0.4	0.4	0.4	
		0.5	0.5	0.5	0.5	
		0.6	0.6	0.6	0.6	
V	V _{IL}	0.1	0.1	0.1	0.1	10V
		0.2	0.2	0.2	0.2	
		0.3	0.3	0.3	0.3	
		0.4	0.4	0.4	0.4	
		0.5	0.5	0.5	0.5	
		0.6	0.6	0.6	0.6	
V	V _{IH}	0.1	0.1	0.1	0.1	10V
		0.2	0.2	0.2	0.2	
		0.3	0.3	0.3	0.3	
		0.4	0.4	0.4	0.4	
		0.5	0.5	0.5	0.5	
		0.6	0.6	0.6	0.6	
V	V _{IS}	0.1	0.1	0.1	0.1	10V
		0.2	0.2	0.2	0.2	
		0.3	0.3	0.3	0.3	
		0.4	0.4	0.4	0.4	
		0.5	0.5	0.5	0.5	
		0.6	0.6	0.6	0.6	
V	V _{OS}	0.1	0.1	0.1	0.1	10V
		0.2	0.2	0.2	0.2	
		0.3	0.3	0.3	0.3	
		0.4	0.4	0.4	0.4	
		0.5	0.5	0.5	0.5	
		0.6	0.6	0.6	0.6	

1. The output should be tested at a time, and the duration of the test should be less than 10 ms.

Advanced CMOS Circuits



TEXAS 
INSTRUMENTS

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FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54ACT11241, 74ACT11241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2957, JULY 1987

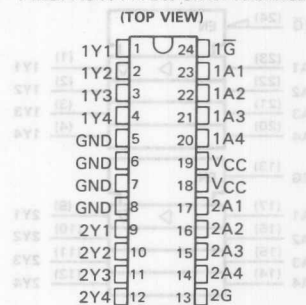
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

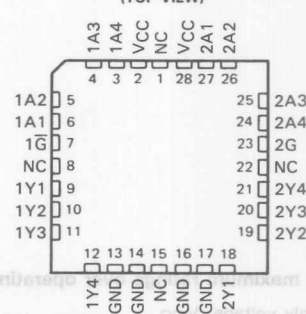
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical \bar{G} (active-low output control) inputs, and complementary G and \bar{G} inputs. These devices feature high fan-out.

The 54ACT11241 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11241 is characterized for operation from -40°C to 85°C.

54ACT11241 ... JT PACKAGE
74ACT11241 ... DW OR NT PACKAGE



54ACT11241 ... FK PACKAGE
(TOP VIEW)



NC—No internal connection

2

Advanced CMOS Circuits

PRODUCT PREVIEW

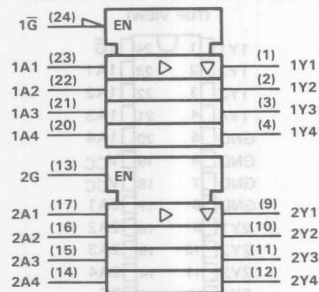
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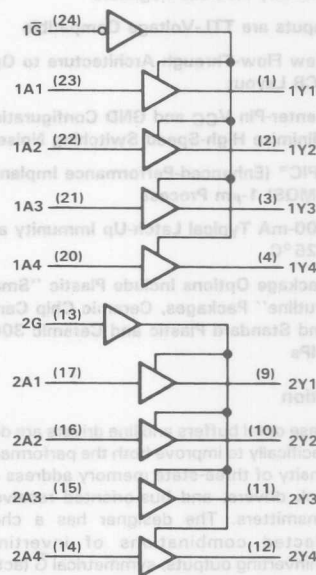
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[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers are for DW, JT, and NT packages.



Pin numbers are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±200 mA
Storage temperature range	−65°C to 150°C

[‡] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54ACT11241, 74ACT11241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	TEST CONDITIONS	54ACT11241		74ACT11241		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
I _{OH}	High-level output current		-24		-24	mA
I _{OL}	Low-level output current		24		24	mA
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
Δt/Δv	Input transition rise or fall rate	0	10	0	10	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11241		74ACT11241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA [†]	5.5 V				1.65				
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±10		±5	μA
	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μA
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.9		1		1	mA
C _i	V _I = V _{CC} or GND	5 V			4					pF
C _o	V _O = V _{CC} or GND	5 V			10					pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics, V_{CC} = 5 V ± 0.5 V (see Figure 1)

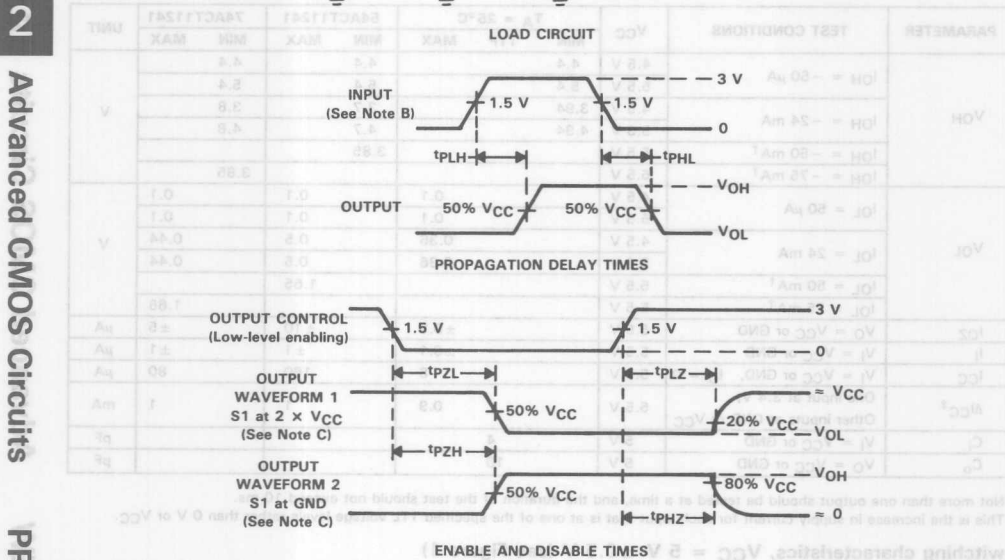
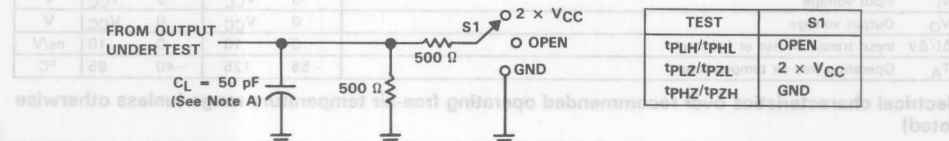
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54ACT11241		74ACT11241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y		7.5						ns
t _{PHL}				6						
t _{PZH}	1 \bar{G}	Y		8.5						
t _{PZL}				7.9						
t _{PHZ}	1 \bar{G}	Y		7.9						
t _{PLZ}				8.6						
t _{PZH}	2 \bar{G}	Y		7.5						
t _{PZL}				7.1						
t _{PHZ}	2 \bar{G}	Y		8						
t _{PLZ}				8.6						

54ACT11241, 74ACT11241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per buffer	Outputs enabled	27	pF
	Outputs disabled	9	

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_0 = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11244, 74AC11244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

MAY 1987

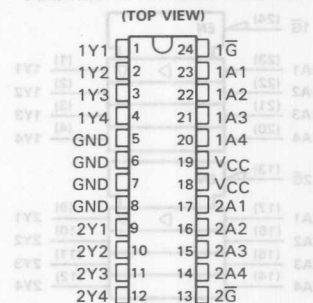
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

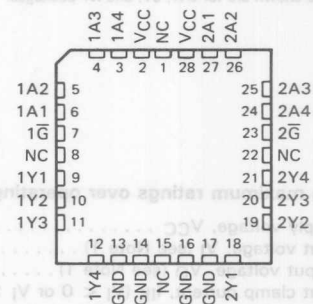
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the AC11240 and AC11241, these devices provide the choice of selected combinations of inverting outputs, symmetrical \bar{G} (active-low output control) inputs, and complementary G and \bar{G} inputs.

The 54AC11244 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74AC11244 is characterized for operation from -40°C to 85°C .

54AC11244 ... JT PACKAGE
74AC11244 ... DW OR NT PACKAGE



54AC11244 ... FK PACKAGE
(TOP VIEW)



NC—No internal connection

2

Advanced CMOS Circuits

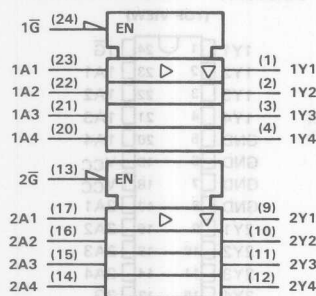
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TEXAS
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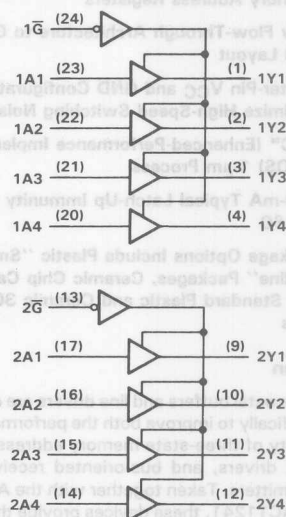
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logic symbol[†]

[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±200 mA
Storage temperature range	−65°C to 150°C

[‡]Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54AC11244, 74AC11244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

			54AC11244			74AC11244			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1			2.1			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 5.5 V	3.85			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V			0.9			0.9	V
		V _{CC} = 4.5 V			1.35			1.35	
		V _{CC} = 5.5 V			1.65			1.65	
I _{OH}	High-level output current	V _{CC} = 3 V			-4			-4	mA
		V _{CC} = 4.5 V			-24			-24	
		V _{CC} = 5.5 V			-24			-24	
I _{OL}	Low-level output current	V _{CC} = 3 V			12			12	mA
		V _{CC} = 4.5 V			24			24	
		V _{CC} = 5.5 V			24			24	
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise or fall rate	Ⓖ	0		5	0		5	ns/V
		Data	0		10	0		10	
T _A	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range, a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11244		74AC11244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA†	5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	3 V		0.1		0.1		0.1		V
		4.5 V		0.1		0.1		0.1		
		5.5 V		0.1		0.1		0.1		
	I _{OL} = 12 mA	3 V		0.36		0.5		0.44		
		4.5 V		0.36		0.5		0.44		
		5.5 V		0.36		0.5		0.44		
	I _{OL} = 50 mA†	5.5 V				1.65				
I _{OZ}	V _O = V _{CC} or GND	5.5 V		±0.5		±10		±5		μA
	V _I = V _{CC} or GND	5.5 V		±0.1		±1		±1		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		8		160		80		μA
C _i	V _I = V _{CC} or GND	5 V		4						pF
C _o	V _O = V _{CC} or GND	5 V		10						pF

†Not more than one output should be tested at one time, and the duration of the test should not exceed 10 ms.

54AC11244, 74AC11244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC RANGE	TA = 25°C			54AC11244		74AC11244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	A	Y	3.3 ± 0.3 V	1.5	7.1	9.3	1.5	10.8	1.5	10.2	ns
			5 ± 0.5 V	1.5	4.9	6.7	1.5	7.7	1.5	7.3	
			3.3 ± 0.3 V	1.5	6.3	8.6	1.5	10.5	1.5	9.5	
tPHL	A	Y	5 ± 0.5 V	1.5	4.5	6.4	1.5	7.4	1.5	6.9	ns
			3.3 ± 0.3 V	1.5	8	10.7	1.5	12.9	1.5	11.8	
			5 ± 0.5 V	1.5	5.4	7.7	1.5	9.3	1.5	8.5	
tPZH	G	Y	3.3 ± 0.3 V	1.5	7.9	10.6	1.5	12.9	1.5	11.9	ns
			5 ± 0.5 V	1.5	5.4	7.6	1.5	9.1	1.5	8.5	
			3.3 ± 0.3 V	1.5	5.9	7.9	1.5	8.7	1.5	8.3	
tPZL	G	Y	5 ± 0.5 V	1.5	5.2	7	1.5	7.6	1.5	7.3	ns
			3.3 ± 0.3 V	1.5	7.2	9.4	1.5	10.4	1.5	9.9	
			5 ± 0.5 V	1.5	5.8	7.8	1.5	8.6	1.5	8.2	

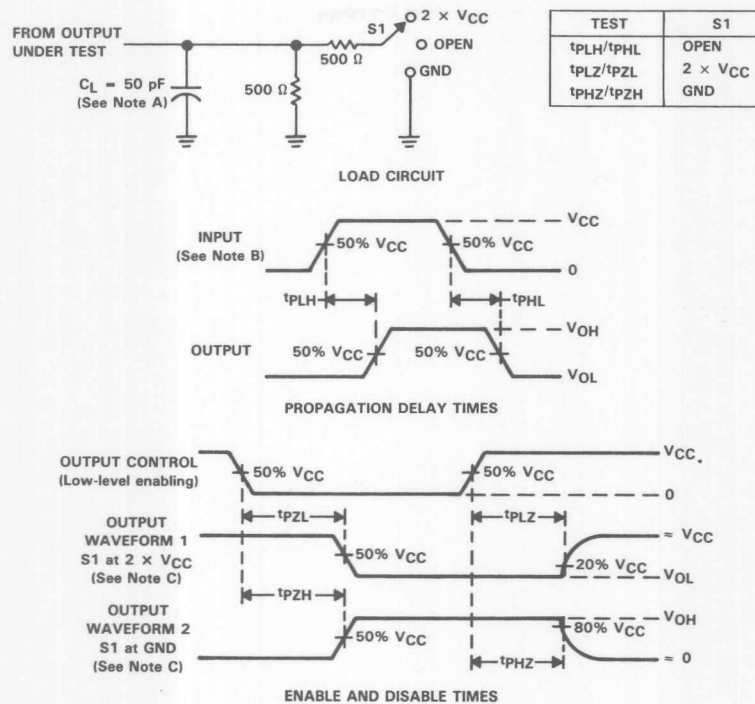
operating characteristics, VCC = 5 V, TA = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
Cpd	Power dissipation capacitance per buffer	Outputs enabled	CL = 50 pF, f = 1 MHz	27	pF
		Outputs disabled		9	

UNIT	VCC RANGE		TA = 25°C		TEST CONDITIONS	PARAMETER
	MAX	MIN	MAX	MIN		
V	3.0	2.0	3.0	2.0	VO = 0.5 V	VO
	4.5	3.5	4.5	3.5	VO = 1.0 V	
	6.0	5.0	6.0	5.0	VO = 1.5 V	
	7.5	6.5	7.5	6.5	VO = 2.0 V	
	9.0	8.0	9.0	8.0	VO = 2.5 V	
	10.5	9.5	10.5	9.5	VO = 3.0 V	
	12.0	11.0	12.0	11.0	VO = 3.5 V	
	13.5	12.5	13.5	12.5	VO = 4.0 V	
V	1.0	0.5	1.0	0.5	VO = 0.5 V	VO
	1.0	0.5	1.0	0.5	VO = 1.0 V	
	1.0	0.5	1.0	0.5	VO = 1.5 V	
	1.0	0.5	1.0	0.5	VO = 2.0 V	
	1.0	0.5	1.0	0.5	VO = 2.5 V	
	1.0	0.5	1.0	0.5	VO = 3.0 V	
	1.0	0.5	1.0	0.5	VO = 3.5 V	
	1.0	0.5	1.0	0.5	VO = 4.0 V	
A	0.5	0.1	0.5	0.1	VO = 0.5 V	VO
	1.0	0.1	1.0	0.1	VO = 1.0 V	
A	0.5	0.1	0.5	0.1	VO = 0.5 V	VO
	1.0	0.1	1.0	0.1	VO = 1.0 V	
A	0.5	0.1	0.5	0.1	VO = 0.5 V	VO
	1.0	0.1	1.0	0.1	VO = 1.0 V	
A	0.5	0.1	0.5	0.1	VO = 0.5 V	VO
	1.0	0.1	1.0	0.1	VO = 1.0 V	

54AC11244, 74AC11244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



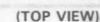
- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

D2957. AUGUST 1987

- description**

The 54ACT11244 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74ACT11244 is characterized for operation from -40°C to 85°C .



(TOP VIEW)



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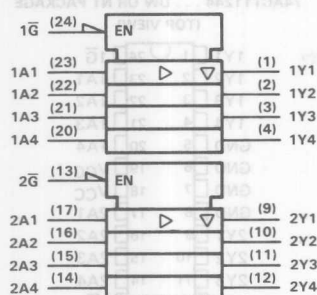


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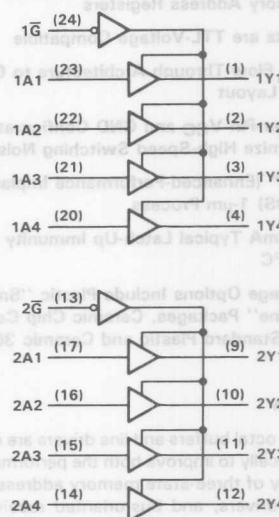
54ACT11244, 74ACT11244

OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

logic symbol†



logic diagram (positive logic)



2

Advanced CMOS Circuits

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	–0.5 V to 7 V
Input voltage, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±200 mA
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

	54ACT11244		74ACT11244		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
I_{OH} High-level output current		–24		–24	mA
I_{OL} Low-level output current		24		24	mA
V_I Input voltage	0	V_{CC}	0	V_{CC}	V
V_O Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$ Input transition rise or fall rate	0	10	0	10	ns/V
T_A Operating free-air temperature	–55	125	–40	85	°C

54ACT11244, 74ACT11244

OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11244		74ACT11244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
V _{OL}	I _{OL} = 50 µA	4.5 V		0.1		0.1		0.1		V
		5.5 V		0.1		0.1		0.1		
	I _{OL} = 24 mA	4.5 V		0.36		0.5		0.44		
		5.5 V		0.36		0.5		0.44		
	I _{OL} = 50 mA [†]	5.5 V				1.65				
	I _{OL} = 75 mA [†]	5.5 V						1.65		
I _{OZ}	V _O = V _{CC} or GND	5.5 V		±0.5		±10		±5		µA
I _I	V _I = V _{CC} or GND	5.5 V		±0.1		±1		±1		µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		8		160		80		µA
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V		0.9		1		1		mA
C _i	V _I = V _{CC} or GND	5 V		4						pF
C _o	V _O = V _{CC} or GND	5 V		10						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics, V_{CC} = 5 V ± 0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54ACT11244		74ACT11244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	1.5	6	8.9	1.5	10.6	1.5	9.9	ns
t _{PHL}			1.5	5.4	8.6	1.5	9.7	1.5	9.2	
t _{PZH}	\bar{A}	Y	1.5	6.6	11.3	1.5	13.4	1.5	12.5	ns
t _{PZL}			1.5	6.7	10.5	1.5	12.2	1.5	11.4	
t _{PHZ}	\bar{A}	Y	1.5	7.4	9.8	1.5	10.8	1.5	10.4	ns
t _{PLZ}			1.5	7.8	10.6	1.5	11.6	1.5	11.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per buffer	Outputs enabled	27	pF
	Outputs disabled	9	

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Advanced CMOS Circuits

54ACT11244, 74ACT11244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

2 Advanced CMOS Circuits

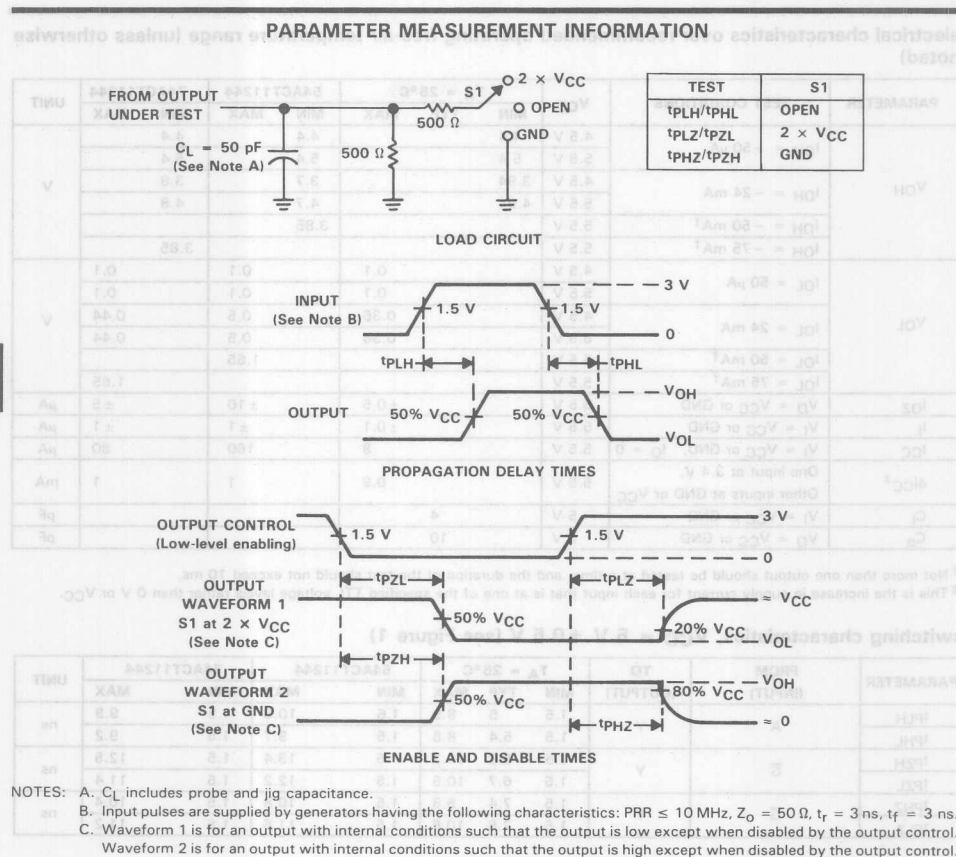


FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

PARAMETER	TEST CONDITIONS	UNIT
t_{PLH}	$C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$	ns
t_{PHL}	$C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$	ns
t_{PZL}	$C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$	ns
t_{PZH}	$C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$	ns

54AC11245, 74AC11245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2957, JULY 1987

- 3-State Outputs Drive Bus Lines Directly
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

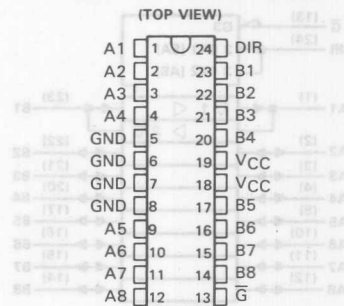
description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

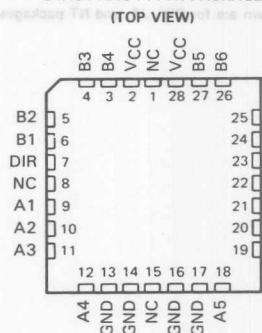
The devices allow data transmission from the A bus to the B bus, or from the B bus to the A bus, depending upon the logic level at the direction control (DIR) input. The enable input (\bar{G}) can be used to disable the device so that the buses are effectively isolated.

The 54AC11245 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC11245 is characterized for operation from -40°C to 85°C.

54AC11245 ... JT PACKAGE
74AC11245 ... DW OR NT PACKAGE



54AC11245 ... FK PACKAGE



NC—No internal connection

FUNCTION TABLE

ENABLE \bar{G}	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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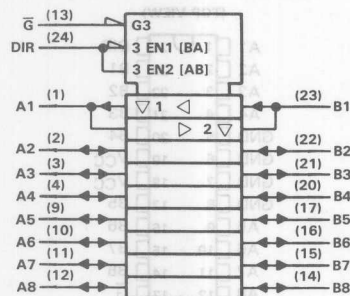
Advanced CMOS Circuits

PRODUCT PREVIEW

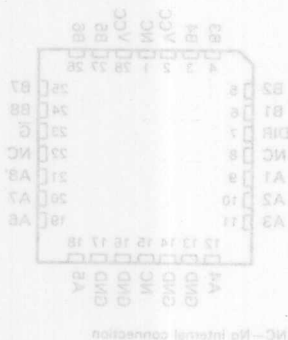
54AC11245, 74AC11245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

1987 JULY 1987

logic symbol†



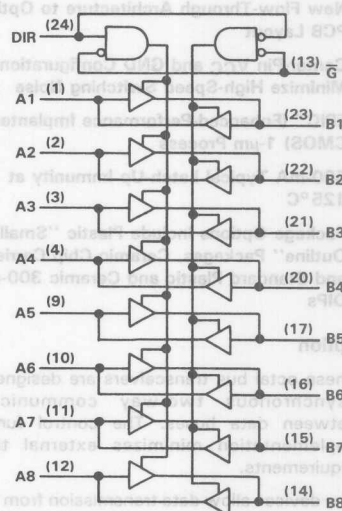
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.



FUNCTION TABLE

ENABLE CONTROL	DIRECTION	OPERATION
L	DIR	B data to A bus
L	H	A data to B bus
H	X	isolation

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages. The enable input (G) can be used to disable the device so that the buses are effectively isolated. The 54AC11245 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC11245 is characterized for operation from -40°C to 85°C.

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Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11245, 74AC11245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54AC11245			74AC11245			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 2)	3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V			2.1			V
		2.1			2.1			
		V _{CC} = 4.5 V			3.15			
V _{IL}	Low-level input voltage	V _{CC} = 5.5 V			3.85			V
		V _{CC} = 3 V			0.9			
		V _{CC} = 4.5 V			1.35			
I _{OH}	High-level output current	V _{CC} = 5.5 V			1.65			mA
		V _{CC} = 3 V			-4			
		V _{CC} = 4.5 V			-24			
I _{OL}	Low-level output current	V _{CC} = 5.5 V			-24			mA
		V _{CC} = 3 V			12			
		V _{CC} = 4.5 V			24			
V _I	Input voltage	0			V _{CC}	0	V _{CC}	V
V _O	Output voltage	0			V _{CC}	0	V _{CC}	V
Δt/Δv	Input transition rise or fall rate	0			10	0	10	ns/V
T _A	Operating free-air temperature	-55			125	-40	85	°C

NOTE 2: No electrical or switching characteristics are specified at $V_{CC} < 3$ V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

54	A	B	C	D	E	F	G	H
74	A	B	C	D	E	F	G	H

UNIT	TYP	TEST CONDITIONS	PARAMETER
dB	84	$C_L = 50$ pF, $f = 1$ MHz	Output enabled
dB	76		Output disabled

54AC11245, 74AC11245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11245		74AC11245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
	I _{OH} = -24 mA	5.5 V	4.94			4.7		4.8		
V _{OL}	I _{OL} = 50 µA	3 V		0.1		0.1		0.1		V
		4.5 V		0.1		0.1		0.1		
		5.5 V		0.1		0.1		0.1		
	I _{OL} = 12 mA	3 V		0.36		0.5		0.44		
		4.5 V		0.36		0.5		0.44		
	I _{OL} = 24 mA	5.5 V		0.36		0.5		0.44		
I _{OZ}	V _O = V _{CC} or GND	3 V			0.1					µA
		4.5 V			0.1					
		5.5 V			0.1					
	I _I = V _I = V _{CC} or GND	3 V		±0.5		±10		±5		
		4.5 V		±0.1		±1		±1		
	I _{CC}	5.5 V		8		160		80		
C _I	V _I = V _{CC} or GND	5 V		4						pF
C _O	V _O = V _{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

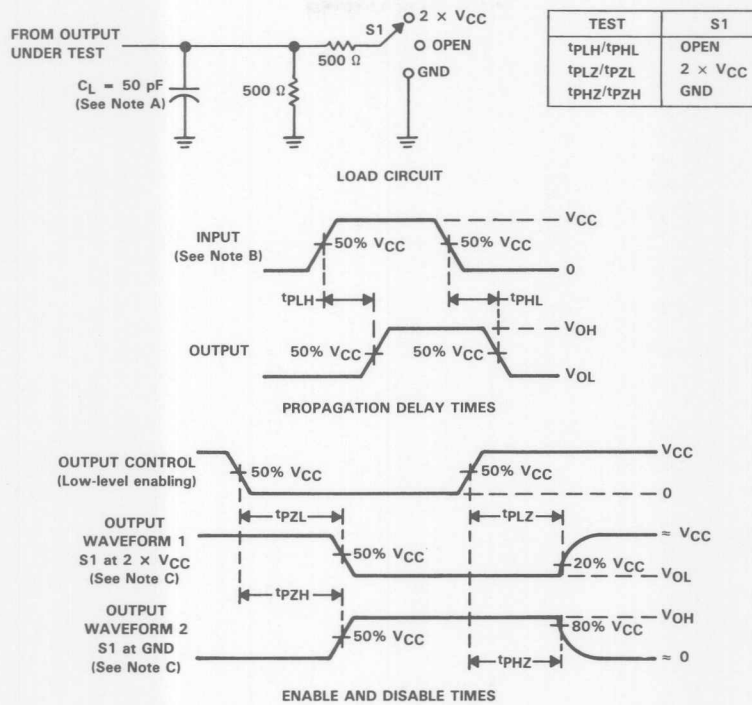
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C			54AC11245		74AC11245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		6.9						
t _{PHL}	A or B	B or A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		6.1						
t _{PZH}	A or B	B or A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		8						
t _{PZL}	A or B	B or A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		8.1						
t _{PHZ}	A or B	B or A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		7.2						
t _{PLZ}	A or B	B or A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		7.6						

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C _L = 50 pF, f = 1 MHz	64	pF
		Outputs disabled		16	

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54ACT11245, 74ACT11245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2957, JULY 1987

- 3-State Outputs Drive Bus Lines Directly
- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

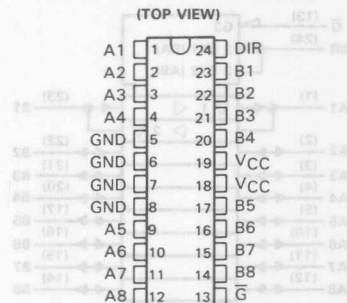
description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

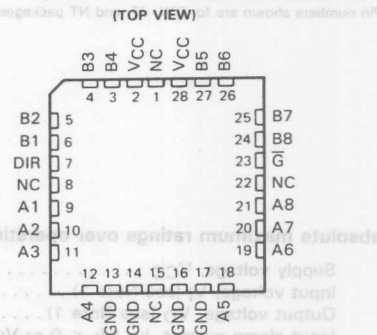
The devices allow data transmission from the A bus to the B bus, or from the B bus to the A bus, depending upon the logic level at the direction control (DIR) input. The enable input (\bar{G}) can be used to disable the device so that the buses are effectively isolated.

The 54ACT11245 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11245 is characterized for operation from -40°C to 85°C.

54ACT11245 ... JT PACKAGE
74ACT11245 ... DW OR NT PACKAGE



54ACT11245 ... FK PACKAGE



NC—No internal connection

FUNCTION TABLE

ENABLE \bar{G}	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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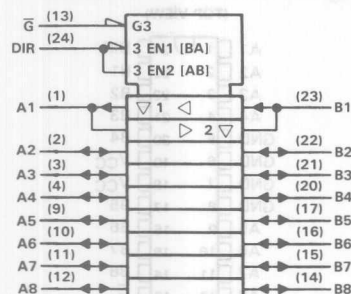
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Advanced CMOS Circuits

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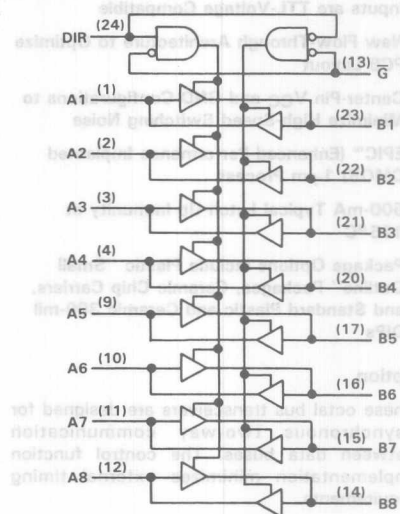
54ACT11245, 74ACT11245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

OPERATION	DIRECTION	ENABLE
	DIR	\bar{E}
all A to all B	L	L
all B to all A	H	L
bidirectional	X	H

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Advanced CMOS Circuits

PRODUCT PREVIEW

54ACT11245, 74ACT11245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	TEST CONDITIONS	54ACT11245		74ACT11245		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
I _{OH}	High-level output current		-24		-24	mA
I _{OL}	Low-level output current		24		24	mA
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
Δt/Δv	Input transition rise or fall rate	0	10	0	10	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11245		74ACT11245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
	I _{OH} = -75 mA [†]	5.5 V						3.85		
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA [†]	5.5 V				1.65				
	I _{OL} = 75 mA [†]	5.5 V						1.65		
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5	±10		±5		μA
I _I	V _I = V _{CC} or GND	5.5 V			±0.1	±1		±1		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8	160		80		μA
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.9	1		1		mA
C _i	V _I = V _{CC} or GND	5 V			4					pF
C _o	V _O = V _{CC} or GND	5 V			10					pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics, V_{CC} = 5 V ± 0.5 V (see Figure 1)

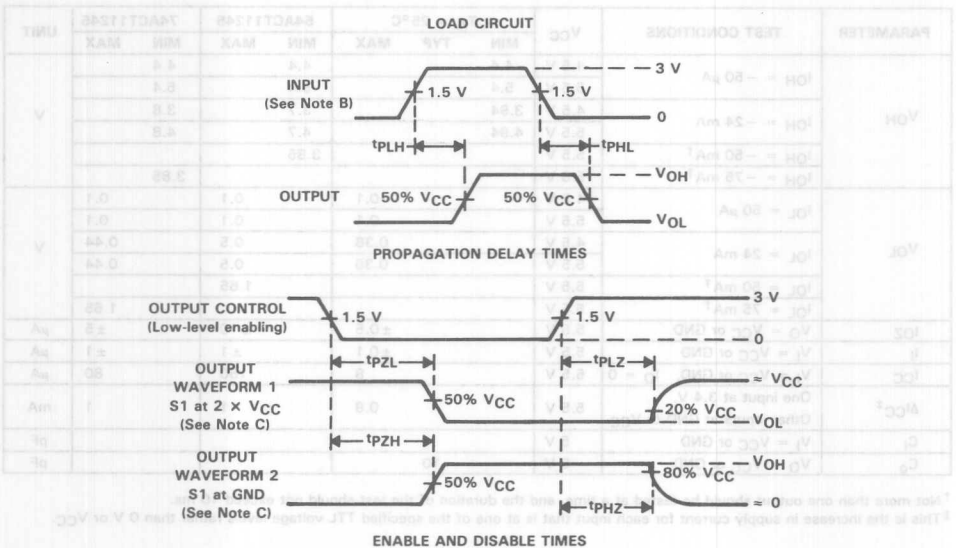
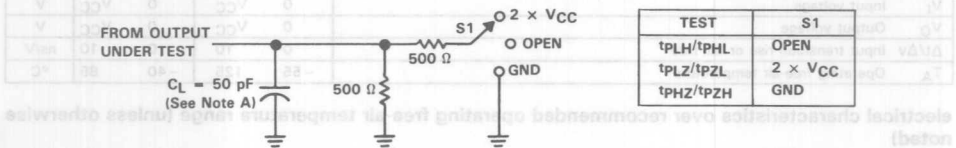
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54ACT11245		74ACT11245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A		5						ns
t _{PHL}				5.9						
t _{PZH}	\bar{G}	A or B		6.6						
t _{PZL}				7.7						
t _{PHZ}	\bar{G}	A or B		8.8						
t _{PLZ}				8.6						

54ACT11245, 74ACT11245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		TYP	UNIT
	Outputs enabled	Outputs disabled	66	pF
C_{pd} Power dissipation capacitance per transceiver	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$		19	

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54AC11373, 74AC11373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

D2957, MAY 1987

- 8 Latches in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

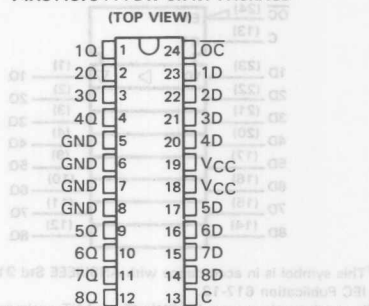
The eight latches of the 'AC11373 are transparent D-type latches. While the enable (C) is high, the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

A buffered output-control input (\overline{OC}) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

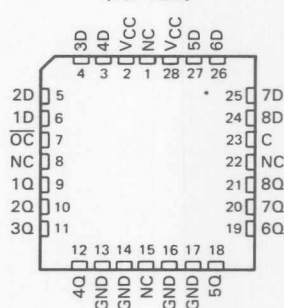
The output control \overline{OC} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The 54AC11373 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74AC11373 is characterized for operation from -40°C to 85°C .

54AC11373 ... JT PACKAGE
74AC11373 ... DW OR NT PACKAGE



54AC11373 ... FK PACKAGE
(TOP VIEW)



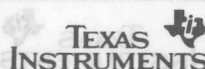
NC—No internal connection

FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
\overline{OC}	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

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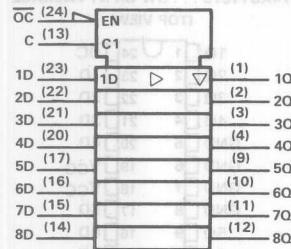
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54AC11373, 74AC11373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

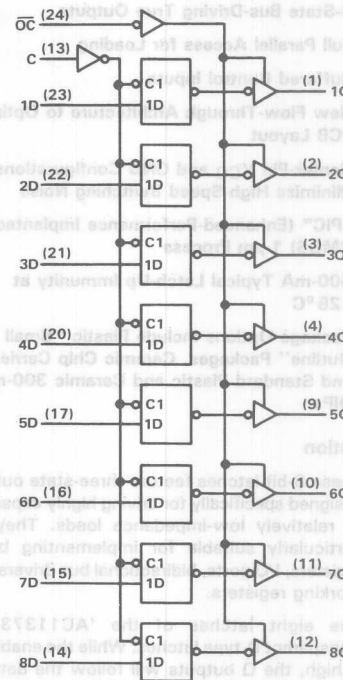
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54AC11373, 74AC11373
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

			54AC11373			74AC11373			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1			2.1			V
		V _{CC} = 4.5 V	3.15			3.15			
V _{IL}	Low-level input voltage	V _{CC} = 3 V			0.9			0.9	V
		V _{CC} = 4.5 V			1.35			1.35	
		V _{CC} = 5.5 V			1.65			1.65	
I _{OH}	High-level output current	V _{CC} = 3 V			-4			-4	mA
		V _{CC} = 4.5 V			-24			-24	
		V _{CC} = 5.5 V			-24			-24	
I _{OL}	Low-level output current	V _{CC} = 3 V			12			12	mA
		V _{CC} = 4.5 V			24			24	
		V _{CC} = 5.5 V			24			24	
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise or fall rate	OC	0		5	0		5	ns/V
		Data	0		10	0		10	
T _A	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range, a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11373		74AC11373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA†	5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA†	5.5 V					1.65			
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±10		±5	μA
	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μA
C _i	V _I = V _{CC} or GND	5 V		4						pF
C _O	V _O = V _{CC} or GND	5 V		10						pF

†Not more than one output should be tested at one time, and the duration of the test should not exceed 10 ms.

54AC11373, 74AC11373
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

timing requirements (see Figure 1)

	V _{CC} RANGE	T _A = 25°C		54AC11373		74AC11373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w Pulse duration, enable C high	3.3 ± 0.3 V	5.5		5.5		5.5		ns
	5 ± 0.5 V	4		4		4		
t _{su} Setup time, data before enable C↓	3.3 ± 0.3 V	4		4		4		ns
	5 ± 0.5 V	3.5		3.5		3.5		
t _h Hold time data after enable C↓	3.3 ± 0.3 V	2		2		2		ns
	5 ± 0.5 V	2		2		2		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

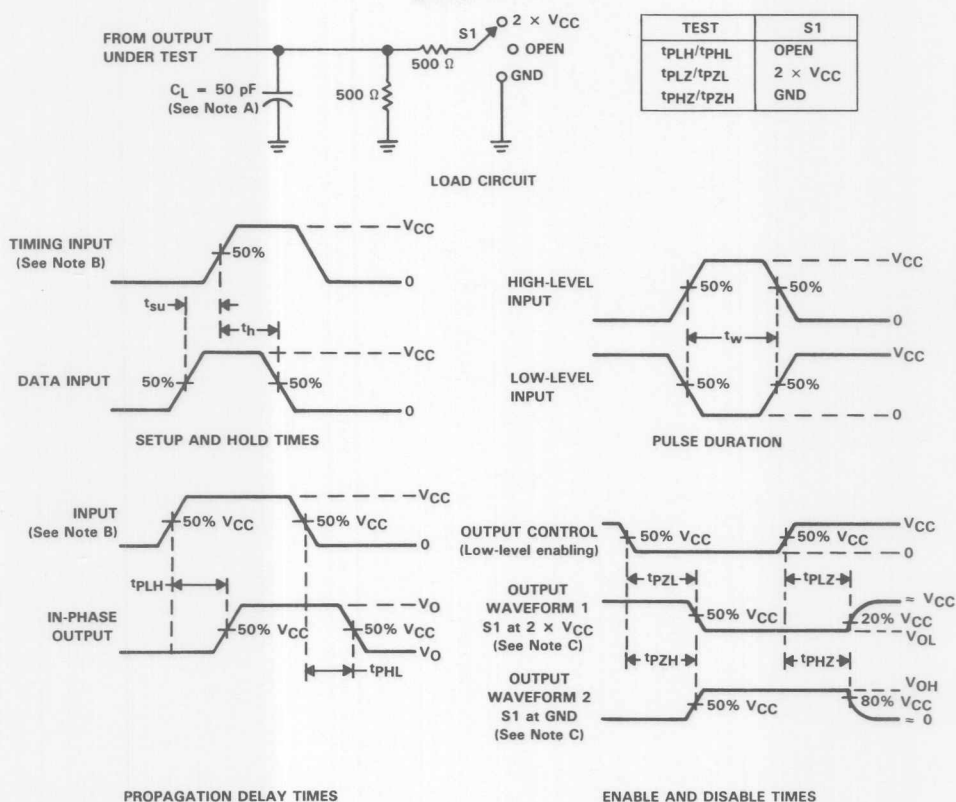
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C			54AC11373		74AC11373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	Q	3.3 ± 0.3 V	1.5	9	13.1	1.5	15.7	1.5	14.8	ns
			5 ± 0.5 V	1.5	6	8.9	1.5	11.1	1.5	10.3	
			3.3 ± 0.3 V	1.5	8	10.6	1.5	12.4	1.5	11.7	
t _{PHL}	C	Any Q	5 ± 0.5 V	1.5	5.5	7.6	1.5	9.1	1.5	8.4	ns
			3.3 ± 0.3 V	1.5	10	14.5	1.5	17.4	1.5	16.3	
			5 ± 0.5 V	1.5	6.5	10	1.5	12.1	1.5	11.3	
t _{PLH}	C	Any Q	3.3 ± 0.3 V	1.5	9.5	12.8	1.5	15.2	1.5	14.2	ns
			5 ± 0.5 V	1.5	6.5	9.1	1.5	11	1.5	10.2	
			3.3 ± 0.3 V	1.5	9	13.1	1.5	15.7	1.5	14.7	
t _{PHL}	C	Any Q	5 ± 0.5 V	1.5	6.5	9.5	1.5	11.6	1.5	10.8	ns
			3.3 ± 0.3 V	1.5	8.5	11.6	1.5	14.1	1.5	13.1	
			5 ± 0.5 V	1.5	6	8.6	1.5	10.9	1.5	9.7	
t _{PZH}	C	Any Q	3.3 ± 0.3 V	1.5	9.5	12	1.5	13.1	1.5	12.7	ns
			5 ± 0.5 V	1.5	8.5	10.6	1.5	11.5	1.5	11.1	
			3.3 ± 0.3 V	1.5	7.5	10.2	1.5	11.3	1.5	10.8	
t _{PZL}	C	Any Q	5 ± 0.5 V	1.5	6	8.2	1.5	9.1	1.5	8.7	ns
			3.3 ± 0.3 V	1.5	7.5	10.2	1.5	11.3	1.5	10.8	
			5 ± 0.5 V	1.5	6	8.2	1.5	9.1	1.5	8.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per latch	Outputs enabled	C _L = 50 pF, f = 1 MHz		47	pF
		Outputs disabled			36	
V _I	1.0	1.0	1.0	V _{CC}	V _{CC}	V
	1.0	1.0	1.0	V _{CC}		
	1.0	1.0	1.0	V _{CC}		
	2.0	2.0	2.0	V _{CC}		
	2.0	2.0	2.0	V _{CC}		
	2.0	2.0	2.0	V _{CC}		
	2.0	2.0	2.0	V _{CC}		
A _Q	2±	01±	30±	V _{CC}	V _{CC}	V
	1±	1±	1.0±	V _{CC}		
A _Q	05	05±	6	V _{CC}	V _{CC}	V
t _Q			±	V _{CC}	V _{CC}	V
t _Q			01	V _{CC}	V _{CC}	V

54AC11373, 74AC11373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

2

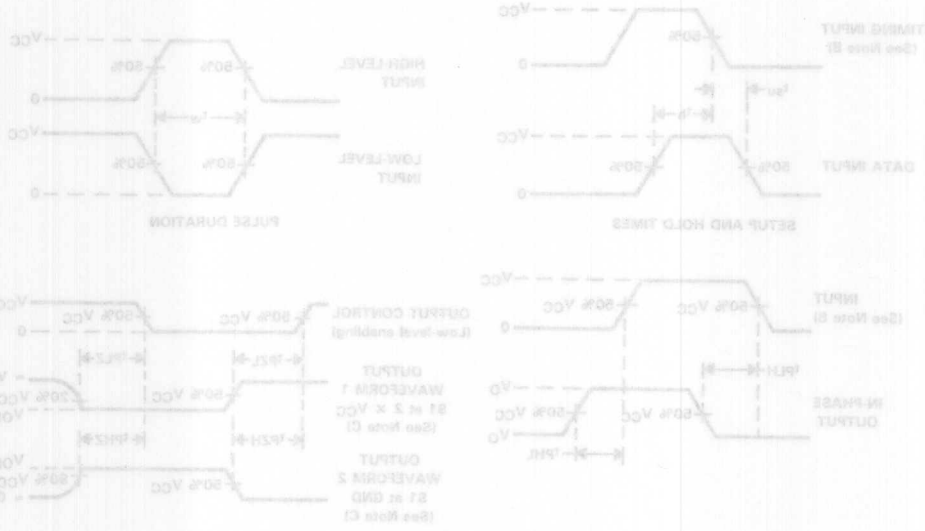
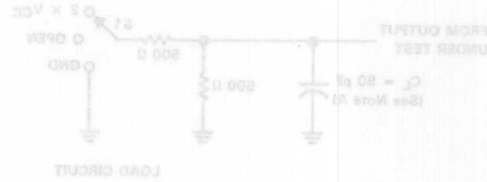
Advanced CMOS Circuits

OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

84AC11373, 74AC11373

PARAMETER MEASUREMENT INFORMATION

TEST	ST
INPUT	OPEN
OUTPUT	3 × V _{CC}
GND	GND



NOTES: A. CL includes probe and its capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR = 10 MHz, 5% = 500 pV, 2 ns, tr = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

ENABLE AND DISABLE TIMES

PROPAGATION DELAY TIMES

54ACT11373, 74ACT11373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

D2957, JUNE 1987

- 8 Latches in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'ACT11373 are transparent D-type latches. While the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

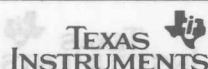
A buffered output-control input (\overline{OC}) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control \overline{OC} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The 54ACT11373 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11373 is characterized for operation from -40°C to 85°C.

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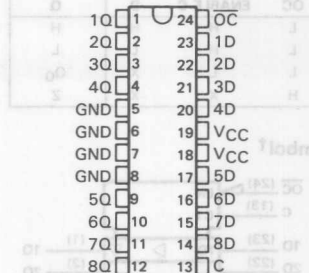
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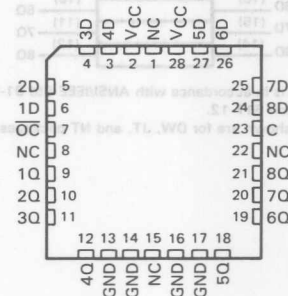
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2-149

54ACT11373 ... JT PACKAGE
74ACT11373 ... DW OR NT PACKAGE
(TOP VIEW)



54ACT11373 ... FK PACKAGE
(TOP VIEW)



NC—No internal connection

2

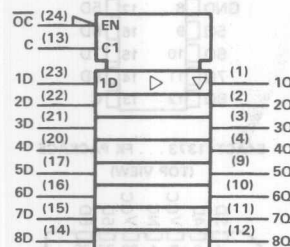
Advanced CMOS Circuits

54ACT11373, 74ACT11373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
\overline{OC}	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

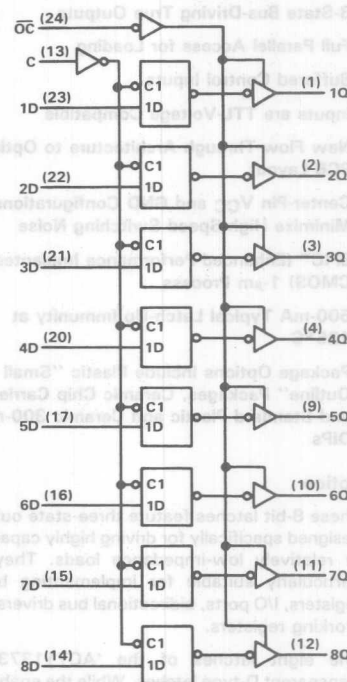
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54ACT11373, 74ACT11373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11373		74ACT11373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		4.5		5.5	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage		2					2		V
V _{IL}	Low-level input voltage				0.8		0.8		0.8	V
I _{OH}	High-level output current					-24		-24		mA
I _{OL}	Low-level output current					24		24		mA
V _I	Input voltage		0		V _{CC}	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage		0		V _{CC}	0	V _{CC}	0	V _{CC}	V
Δt/Δv	Input transition rise or fall rate		0		10	0	10	0	10	ns/V
T _A	Operating free-air temperature		-55		125	-40	85			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11373		74ACT11373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA [†]	5.5 V				1.65				
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±10		±5	μA
		5.5 V			±0.1		±1		±1	
	I _I = V _{CC} or GND	5.5 V								
		5.5 V								
	I _{CC}	5.5 V			8		160		80	
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.9		1		1	mA
C _i	V _I = V _{CC} or GND	5 V			4					pF
C _o	V _O = V _{CC} or GND	5 V			10					pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements, V_{CC} = 5 ± 0.5 V (see Figure 1)

PARAMETER	TEST CONDITIONS	T _A = 25°C		54ACT11373		74ACT11373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration, enable C high	5		5		5		ns
t _{su}	Setup time, data before enable C↓	3.5		3.5		3.5		ns
t _h	Hold time data after enable C↓	3.5		3.5		3.5		ns

54ACT11373, 74ACT11373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see Figure 1)

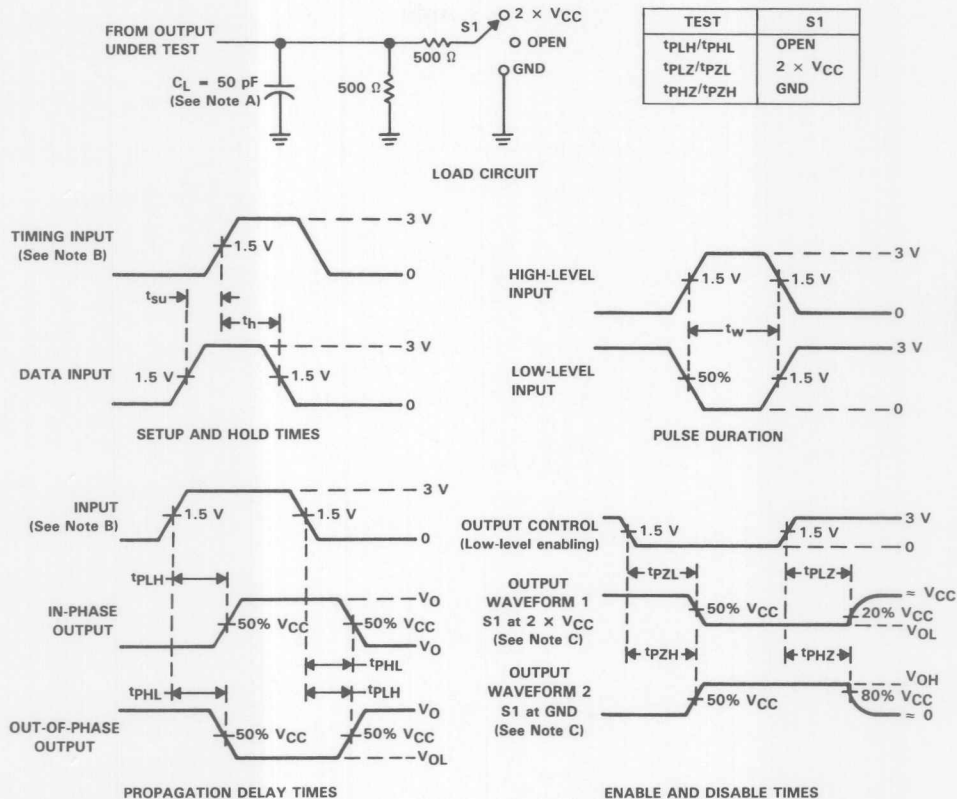
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11373		74ACT11373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.5	7.5	10.3	1.5	12.7	1.5	11.8	ns
t_{PHL}			1.5	6.5	9.3	1.5	10.6	1.5	10	
t_{PLH}	C	Any Q	1.5	8.5	11.3	1.5	14.1	1.5	13	ns
t_{PHL}			1.5	8.5	10.9	1.5	13	1.5	12.2	
t_{PZH}	\overline{OC}	Any Q	1.5	7	10.7	1.5	13.6	1.5	12.5	ns
t_{PZL}			1.5	7.5	10.9	1.5	12.9	1.5	12	
t_{PHZ}	\overline{OC}	Any Q	1.5	10	12.1	1.5	12.7	1.5	12.5	ns
t_{PLZ}			1.5	7.5	9.5	1.5	10.5	1.5	10.1	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS			TYP	UNIT		
C _{pd}	Power dissipation capacitance per latch	Outputs enabled	C _L = 50 pF, f = 1 MHz			65	pF		
		Outputs disabled				54			
V	MAX	MIN	MAX	MIN	MAX	MIN	HGV		
	MIN	MAX	MIN	MAX	MIN	MAX			
	MAX	MIN	MAX	MIN	MAX	MIN			
	MIN	MAX	MIN	MAX	MIN	MAX			
	MAX	MIN	MAX	MIN	MAX	MIN			
	MIN	MAX	MIN	MAX	MIN	MAX			
V	MAX	MIN	MAX	MIN	MAX	MIN	JOL		
	MIN	MAX	MIN	MAX	MIN	MAX			
	MAX	MIN	MAX	MIN	MAX	MIN			
	MIN	MAX	MIN	MAX	MIN	MAX			
	MAX	MIN	MAX	MIN	MAX	MIN			
	MIN	MAX	MIN	MAX	MIN	MAX			
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
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A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
A _{OL}	MIN	MAX	MIN	MAX	MIN				

54ACT11373, 74ACT11373
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54AC11374, 74AC11374 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2957, JULY 1987

- 8 D-Type Flip-Flops in a Single Package
- High-Current 3-State True Outputs Can Drive Up to 15 LSTTL Loads
- Full Parallel Access for Loading
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

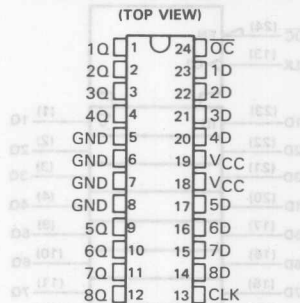
The eight flip-flops of the 'AC11374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic levels that were set up at the D inputs.

An output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

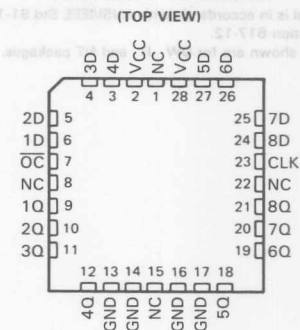
The output control (\overline{OC}) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 54AC11374 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74AC11374 is characterized for operation from -40°C to 85°C .

54AC11374 . . . JT PACKAGE
74AC11374 . . . DW OR NT PACKAGE



54AC11374 . . . FK PACKAGE



NC—No internal connection

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OC}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

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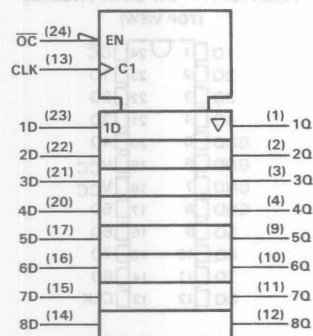
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Advanced CMOS Circuits

PRODUCT PREVIEW

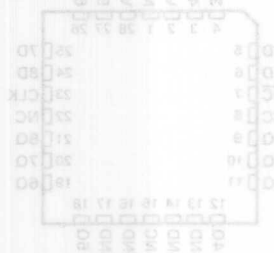
54AC11374, 74AC11374 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

logic symbol†

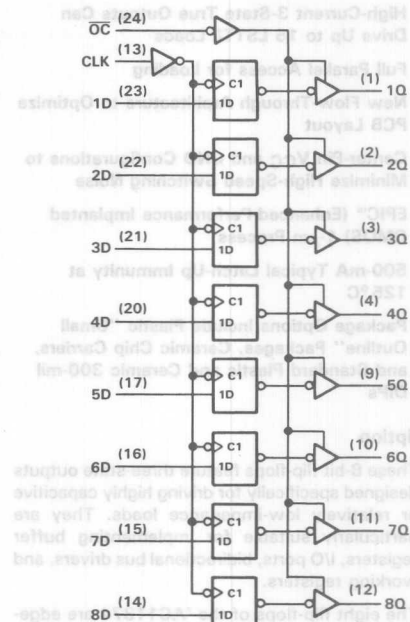


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.



logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11374, 74AC11374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	TEST CONDITIONS	V _{CC}	54AC11374			74AC11374			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1			2.1			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 5.5 V	3.85			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V			0.9			0.9	V
		V _{CC} = 4.5 V			1.35			1.35	
		V _{CC} = 5.5 V			1.65			1.65	
I _{OH}	High-level output current	V _{CC} = 3 V			-4			-4	mA
		V _{CC} = 4.5 V			-24			-24	
		V _{CC} = 5.5 V			-24			-24	
I _{OL}	Low-level output current	V _{CC} = 3 V			12			12	mA
		V _{CC} = 4.5 V			24			24	
		V _{CC} = 5.5 V			24			24	
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise or fall rate		0		10	0		10	ns/V
T _A	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11374		74AC11374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA†	5.5 V				3.85				
	I _{OH} = -75 mA†	5.5 V						3.85		
V _{OL}	I _{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA†	5.5 V					1.65			
	I _{OL} = 75 mA†	5.5 V						1.65		
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±10		±5	μA
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μA
C _i	V _I = V _{CC} or GND	5 V		4						pF
C _o	V _O = V _{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

54AC11374, 74AC11374 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

timing requirements (see Figure 1)

		V _{CC} RANGE	T _A = 25°C		54AC11374		74AC11374		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	3.3 ± 0.3 V	0	100	0	100	0	100	MHz
t _w	Pulse duration	3.3 ± 0.3 V	0	125	0	125	0	125	ns
		5 ± 0.5 V	4		4		4		
t _{su}	Setup time data before CLK↑	3.3 ± 0.3 V	5		5		5		ns
t _h	Hold time data after CLK↑	3.3 ± 0.3 V	4		4		4		ns
		5 ± 0.5 V	5		5		5		
		5 ± 0.5 V	3.5		3.5		3.5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C			54AC11374		74AC11374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	CLK	Any Q	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.3						
t _{PHL}	CLK	Any Q	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.9						
t _{PZH}	OC	Any Q	3.3 ± 0.3 V								ns
			5 ± 0.5 V		4.4						
t _{PZL}	OC	Any Q	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.2						
t _{PHZ}	OC	Any Q	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.8						
t _{PLZ}	OC	Any Q	3.3 ± 0.3 V								ns
			5 ± 0.5 V		4.9						

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C _L = 50 pF, f = 1 MHz		75	pF
		Outputs disabled			66	

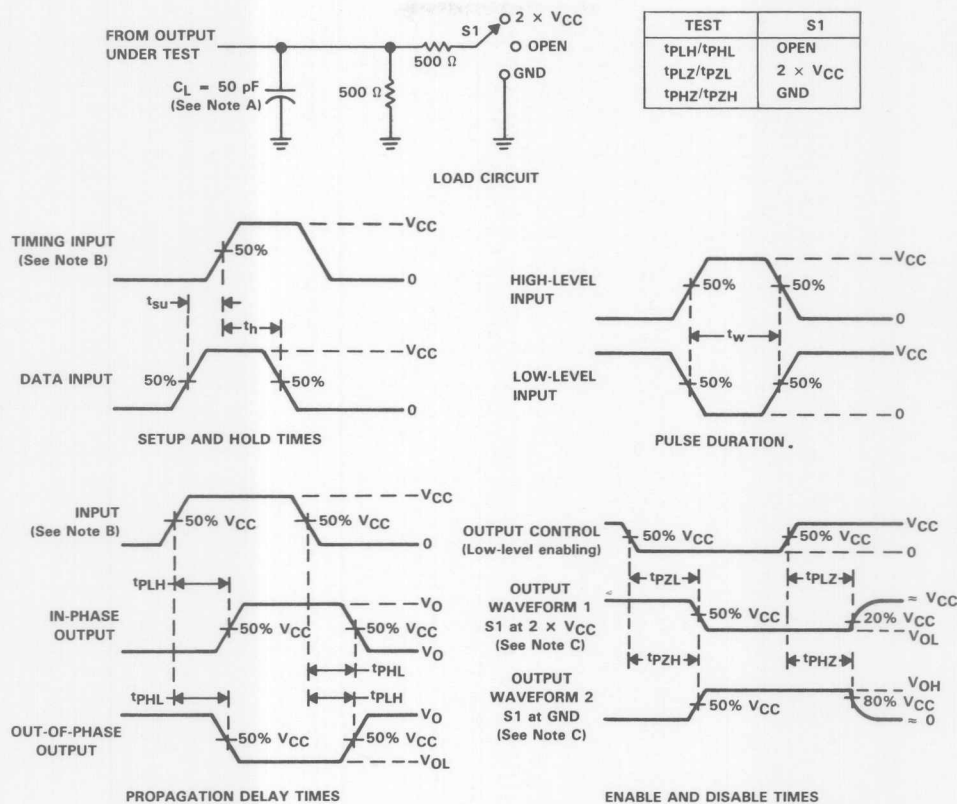
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Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11374, 74AC11374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
For testing f_{MAX} and pulse duration: $t_r = 1$ to 3 ns , $t_f = 1$ to 3 ns .
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS
24AC1137A, 24AC1137B

PARAMETER MEASUREMENT INFORMATION

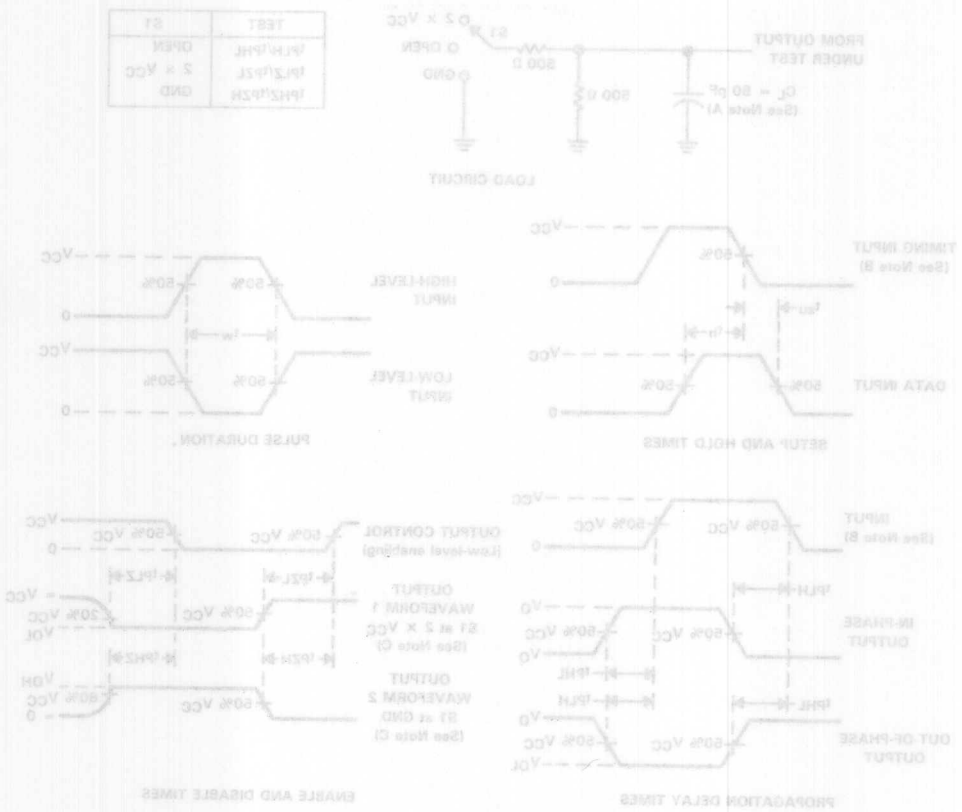


FIGURE 7. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $t_r = 20 \text{ ns}$, $t_f = 3 \text{ ns}$, $t_d = 3 \text{ ns}$.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
D. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. The outputs are measured one at a time with one input transition per measurement.

54ACT11374, 74ACT11374 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2957, JULY 1987

- 8 D-Type Flip-Flops in a Single Package
- High-Current 3-State True Outputs Can Drive Up to 15 LSTTL Loads
- Full Parallel Access for Loading
- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ACT11374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic levels that were set up at the D inputs.

An output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control (\overline{OC}) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

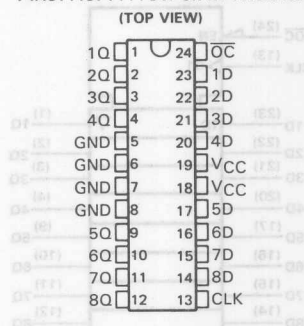
The 54ACT11374 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11374 is characterized for operation from -40°C to 85°C.

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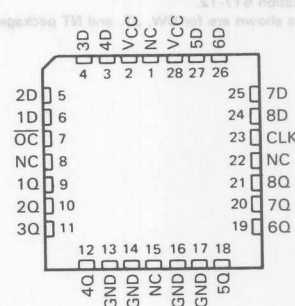
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54ACT11374 . . . JT PACKAGE
74ACT11374 . . . DW OR NT PACKAGE



54ACT11374 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OC}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

2

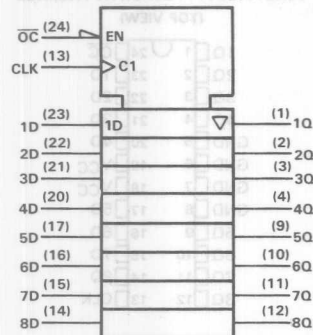
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54ACT11374, 74ACT11374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS

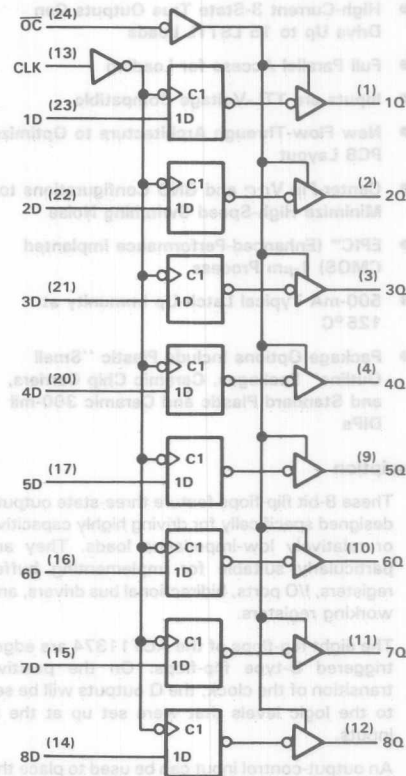
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

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Advanced CMOS Circuits

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54ACT11374, 74ACT11374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	TEST CONDITIONS	T _A = 25°C			54ACT11374		74ACT11374		UNIT
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5		5.5	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2					2		V
V _{IL}	Low-level input voltage			0.8		0.8		0.8	V
I _{OH}	High-level output current			-24		-24		-24	mA
I _{OL}	Low-level output current			24		24		24	mA
V _I	Input voltage	0	V _{CC}		0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}		0	V _{CC}	0	V _{CC}	V
Δt/Δv	Input transition rise or fall rate	0	10		0	10	0	10	ns/V
T _A	Operating free-air temperature	-55	125		-40	85			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11374		74ACT11374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA†	5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	4.5 V		0.1		0.1		0.1		V
		5.5 V		0.1		0.1		0.1		
	I _{OL} = 24 mA	4.5 V		0.36		0.5		0.44		
		5.5 V		0.36		0.5		0.44		
	I _{OL} = 50 mA†	5.5 V				1.65				
I _{OZ}	V _O = V _{CC} or GND	4.5 V								μA
		5.5 V								
	V _I = V _{CC} or GND	5.5 V		±0.1		±1		±1		
		5.5 V		±0.1		±1		±1		
	I _{CC} ‡	5.5 V		8		160		80		
ΔI _{CC} ‡	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V		0.9		1		1		mA
C _i	V _I = V _{CC} or GND	5 V		4						pF
C _o	V _O = V _{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements, V_{CC} = 5 ± 0.5 V (see Figure 1)

PARAMETER	TEST CONDITIONS	T _A = 25°C		54ACT11374		74ACT11374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, enable C high							ns
t _{su}	Setup time, data before enable C ↓							ns
t _h	Hold time data after enable C ↓							ns

54ACT11374, 74ACT11374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11374		74ACT11374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	5.6							ns
t_{PHL}			6.7							
t_{pZH}	\overline{OC}	Any Q	5.6							ns
t_{pZL}			6.7							
t_{PHZ}	\overline{OC}	Any Q	7.3							ns
t_{PLZ}			6.3							

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$		107	pF
		Outputs disabled			96	

2

Advanced CMOS Circuits

PRODUCT PREVIEW

PARAMETER	TEST CONDITIONS		$T_A = 25^\circ\text{C}$			V_{CC}	UNIT
	MIN	MAX	MIN	TYP	MAX		
V_{OH}	$I_{OH} = -20\text{ }\mu\text{A}$		2.4			2.4	V
	$I_{OH} = -50\text{ }\mu\text{A}$		2.3			2.3	
	$I_{OH} = -100\text{ }\mu\text{A}$		2.2			2.2	
	$I_{OH} = -200\text{ }\mu\text{A}$		2.1			2.1	
	$I_{OH} = -400\text{ }\mu\text{A}$		2.0			2.0	
	$I_{OH} = -800\text{ }\mu\text{A}$		1.9			1.9	
V_{OL}	$I_{OL} = 20\text{ }\mu\text{A}$		0.1			0.1	V
	$I_{OL} = 50\text{ }\mu\text{A}$		0.1			0.1	
	$I_{OL} = 100\text{ }\mu\text{A}$		0.1			0.1	
	$I_{OL} = 200\text{ }\mu\text{A}$		0.1			0.1	
	$I_{OL} = 400\text{ }\mu\text{A}$		0.1			0.1	
	$I_{OL} = 800\text{ }\mu\text{A}$		0.1			0.1	
V_{T1}	$V_{CC} = V_{CC} \text{ or } GND$		± 0.5			± 0.5	V
V_{T2}	$V_{CC} = V_{CC} \text{ or } GND$		± 0.5			± 0.5	V
V_{T3}	$V_{CC} = V_{CC} \text{ or } GND$		± 0.5			± 0.5	V
V_{T4}	$V_{CC} = V_{CC} \text{ or } GND$		± 0.5			± 0.5	V
V_{T5}	$V_{CC} = V_{CC} \text{ or } GND$		± 0.5			± 0.5	V
V_{T6}	$V_{CC} = V_{CC} \text{ or } GND$		± 0.5			± 0.5	V
V_{T7}	$V_{CC} = V_{CC} \text{ or } GND$		± 0.5			± 0.5	V
V_{T8}	$V_{CC} = V_{CC} \text{ or } GND$		± 0.5			± 0.5	V

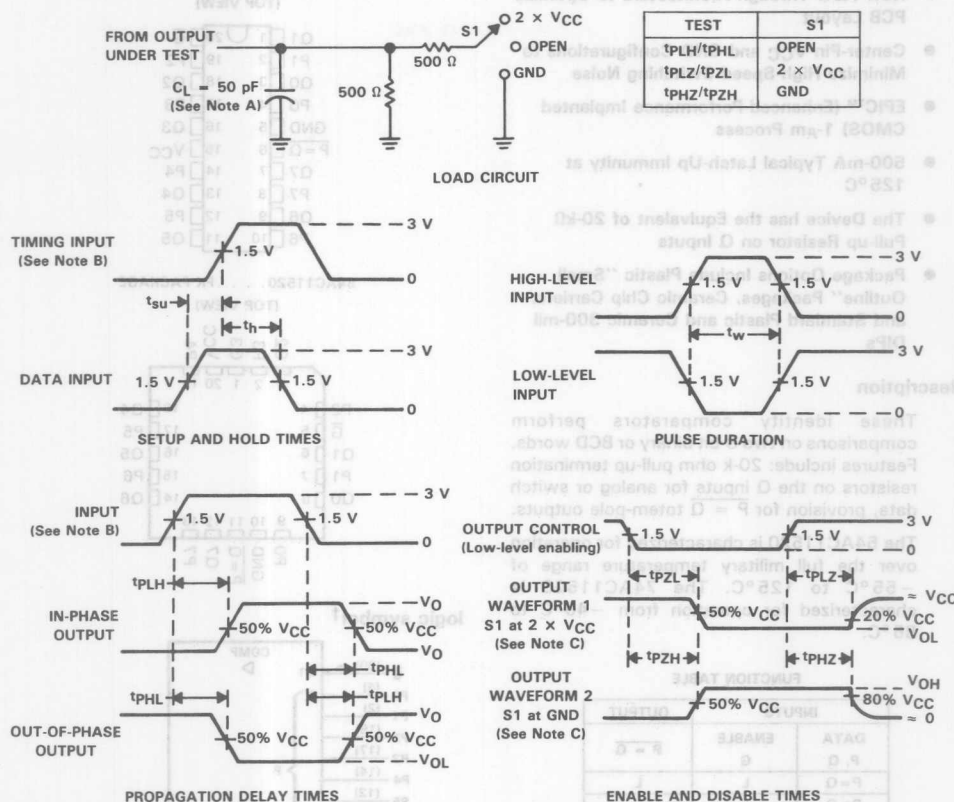
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

Timing requirements, $V_{CC} = 5 \pm 0.5\text{ V}$ (see Figure 1)

UNIT	$T_A = 25^\circ\text{C}$		54ACT11374		74ACT11374	
	MIN	MAX	MIN	MAX	MIN	MAX
t_{PLH}						
t_{PHL}						
t_{pZH}						
t_{pZL}						
t_{PHZ}						
t_{PLZ}						

54ACT11374, 74ACT11374 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_0 = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$. For testing f_{max} and pulse duration: $t_r = 1$ to 3 ns , $t_f = 1$ to 3 ns .
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54AC11520, 74AC11520 8-BIT IDENTITY COMPARATORS

D2957, JULY 1987—REVISED AUGUST 1987

- Compares Two 8-Bit Words
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- The Device has the Equivalent of 20-k Ω Pull-up Resistor on Q Inputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These identity comparators perform comparisons on two 8-bit binary or BCD words. Features include: 20-k ohm pull-up termination resistors on the Q inputs for analog or switch data, provision for $P = Q$ totem-pole outputs.

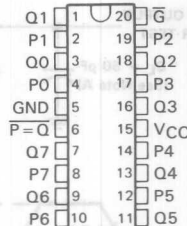
The 54AC11520 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC11520 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE G	$P = Q$
$P = Q$	L	L
$P > Q$	L	H
$P < Q$	L	H
X	H	H

54AC11520 . . . J PACKAGE
74AC11520 . . . DW OR N PACKAGE

(TOP VIEW)

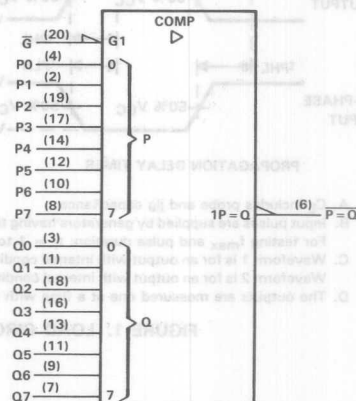


54AC11520 . . . FK PACKAGE

(TOP VIEW)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

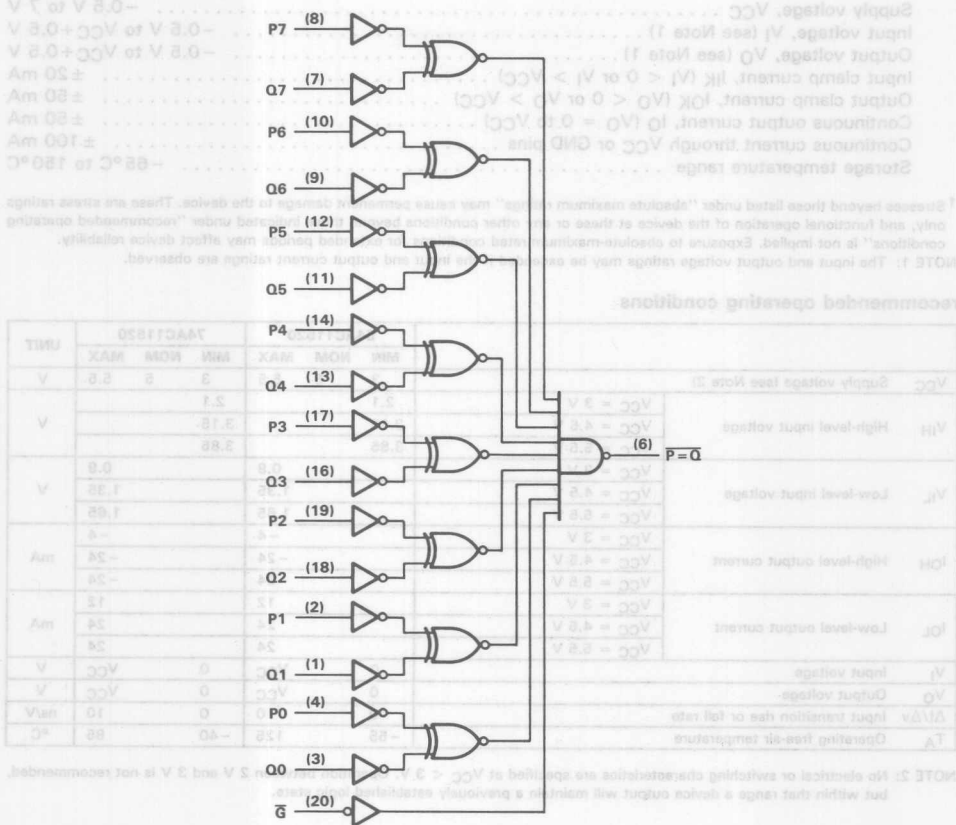
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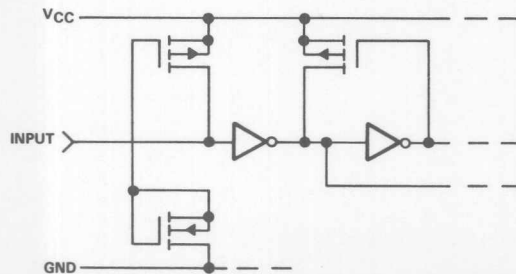
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54AC11520, 74AC11520 8-BIT IDENTITY COMPARATORS

logic diagram (positive logic)



schematic of Q inputs



54AC11520, 74AC11520 8-BIT IDENTITY COMPARATORS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to $V_{CC}+0.5$ V
Output voltage, V_O (see Note 1)	−0.5 V to $V_{CC}+0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	−65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

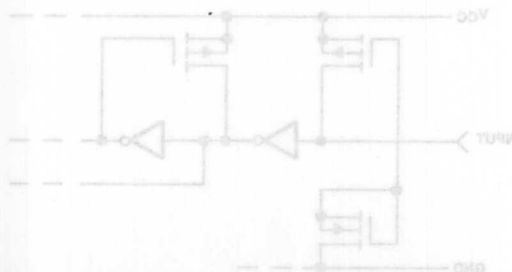
recommended operating conditions

		54AC11520			74AC11520			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)	3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3$ V		2.1	$V_{CC} = 3$ V		2.1	V
		$V_{CC} = 4.5$ V		3.15	$V_{CC} = 4.5$ V		3.15	
		$V_{CC} = 5.5$ V		3.85	$V_{CC} = 5.5$ V		3.85	
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V		0.9	$V_{CC} = 3$ V		0.9	V
		$V_{CC} = 4.5$ V		1.35	$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 5.5$ V		1.65	$V_{CC} = 5.5$ V		1.65	
I_{OH}	High-level output current	$V_{CC} = 3$ V		−4	$V_{CC} = 3$ V		−4	mA
		$V_{CC} = 4.5$ V		−24	$V_{CC} = 4.5$ V		−24	
		$V_{CC} = 5.5$ V		−24	$V_{CC} = 5.5$ V		−24	
I_{OL}	Low-level output current	$V_{CC} = 3$ V		12	$V_{CC} = 3$ V		12	mA
		$V_{CC} = 4.5$ V		24	$V_{CC} = 4.5$ V		24	
		$V_{CC} = 5.5$ V		24	$V_{CC} = 5.5$ V		24	
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at $V_{CC} < 3$ V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

2

Advanced CMOS Circuits



54AC11520, 74AC11520
8-BIT IDENTITY COMPARATORS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11520		74AC11520		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	3 V	2.9	2.9		2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
	I _{OH} = -24 mA	5.5 V	4.94			4.7		4.8		
		5.5 V				3.85				
V _{OL}	I _{OL} = 50 µA	3 V		0.1		0.1		0.1		V
		4.5 V		0.1		0.1		0.1		
		5.5 V		0.1		0.1		0.1		
	I _{OL} = 12 mA	3 V		0.36		0.5		0.44		
		4.5 V		0.36		0.5		0.44		
	I _{OL} = 24 mA	5.5 V		0.36		0.5		0.44		
		5.5 V				1.65				
I _{OZ}	V _O = V _{CC} or GND	3 V								µA
		4.5 V								
		5.5 V								
	I _{IH} V _I = V _{CC} , Q inputs only	3 V								
		4.5 V								
	I _{IL} V _I = GND, Q inputs only	3 V								
		4.5 V								
I _{CC}	V _I = V _{CC} or GND, P and \bar{Q} inputs only	3 V								mA
		4.5 V								
		5.5 V								
	Q inputs at GND	3 V								
		4.5 V								
	Other inputs V _I = V _{CC} or GND	3 V								
		4.5 V								
C _i	V _I = V _{CC} or GND	3 V								pF
		4.5 V								

†Not more than one output or input should be tested at a time and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25 °C			54AC11520		74AC11520		UNIT		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t _{PLH}	P or Q	$\overline{P} = \overline{Q}$	3.3 ± 0.3 V	1.5	12	16.5	1.5	20.1	1.5	18.6	ns		
			5 ± 0.5 V	1.5	8.1	11.1	1.5	13.7	1.5	12.6			
t _{PHL}			\overline{Q}	$\overline{P} = \overline{Q}$	3.3 ± 0.3 V	1.5	10.4	14.4	1.5	17.6	1.5	16.3	ns
					5 ± 0.5 V	1.5	7.1	10.1	1.5	12.3	1.5	11.3	
t _{PLH}	\overline{Q}	$\overline{P} = \overline{Q}$			3.3 ± 0.3 V	1.5	6.9	9	1.5	10.8	1.5	10	ns
					5 ± 0.5 V	1.5	4.9	6.6	1.5	8	1.5	7.4	
t _{PHL}			\overline{Q}	$\overline{P} = \overline{Q}$	3.3 ± 0.3 V	1.5	6.3	8.6	1.5	10.2	1.5	9.5	ns
					5 ± 0.5 V	1.5	4.8	7.1	1.5	8.2	1.5	7.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	C _L = 50 pF, f = 1 MHz	42	pF

2 Advanced CMOS Circuits

FIGURE 2

54ACT11520, 74ACT11520 8-BIT IDENTITY COMPARATORS

D2957, JULY 1987—REVISED AUGUST 1987

- Compares Two 8-Bit Words
- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- The Device has the Equivalent of 20 k Ω Pull-up Resistors on Q Inputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

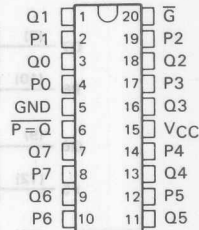
These identity comparators perform comparisons on two 8-bit binary or BCD words. Features include: 20-k ohm pull-up termination resistors on the Q inputs for analog or switch data, provision for $P = \bar{Q}$ totem-pole outputs.

The 54ACT11520 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11520 is characterized for operation from -40°C to 85°C.

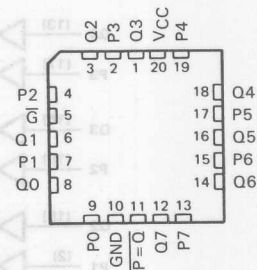
FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE G	$P = \bar{Q}$
$P = Q$	L	L
$P > Q$	L	H
$P < Q$	L	H
X	H	H

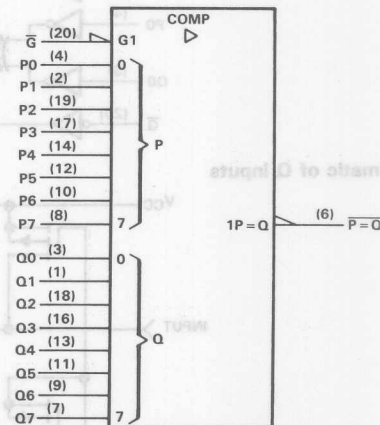
54ACT11520 . . . J PACKAGE
74ACT11520 . . . DW OR N PACKAGE
(TOP VIEW)



54ACT11520 . . . FK PACKAGE
(TOP VIEW)



logic symbol†



EPIC is a trademark of Texas Instruments Incorporated.

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

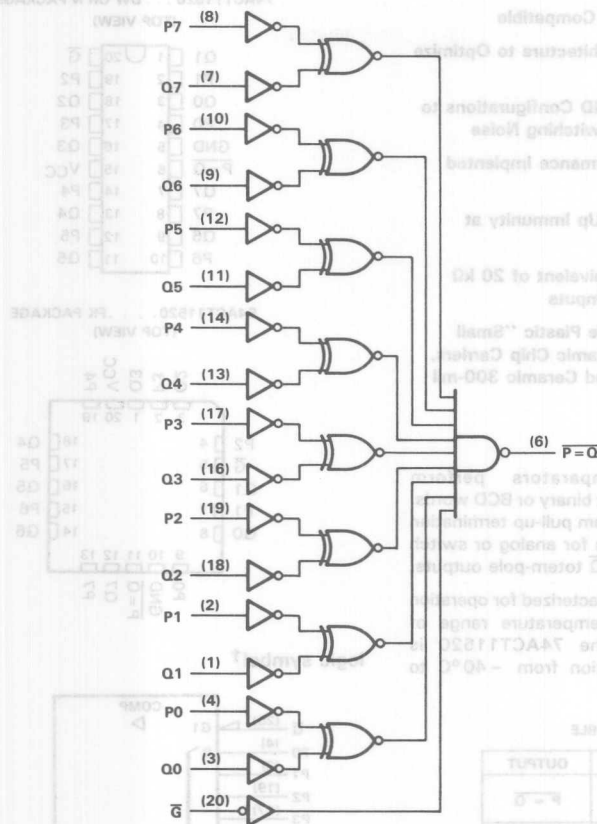
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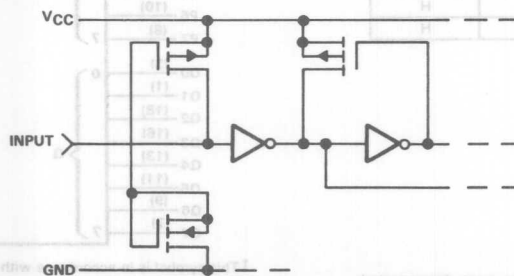
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54ACT11520, 74ACT11520 8-BIT IDENTITY COMPARATORS

logic diagram (positive logic)



schematic of Q inputs



FUNCTION TABLE		
DATA	ENABLE	OUTPUT
P=Q	H	H
P<Q	L	L
P>Q	L	L
P=Q	L	L
X	H	X

2 Advanced CMOS Circuits

54ACT11520, 74ACT11520 8-BIT IDENTITY COMPARATORS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	−65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11520			74ACT11520			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta V$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

2 Advanced CMOS Circuits

switching characteristics $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (see Figure 1)

UNIT	74ACT11520		54ACT11520		$T_A = -55^\circ\text{C}$		TO (OUTPUT)	FROM (INPUT)	PARAMETER
	MAX	MIN	MAX	MIN	MAX	MIN			
ns	14.3	1.8	15.4	1.8	15.7	8.8	1.8	1.8	t_{PLH}
ns	13.9	1.8	15.1	1.8	15.4	8.8	1.8	1.8	t_{PLL}
ns	8.8	1.8	10.3	1.8	8.8	1.8	1.8	1.8	t_{PHL}
ns	8.8	1.8	10.4	1.8	8.8	1.8	1.8	1.8	t_{PHL}

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = -55^\circ\text{C}$

PARAMETER	TEST CONDITIONS	UNIT
C_{in} Input capacitance	$C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$	40 pF

54ACT11520, 74ACT11520 8-BIT IDENTITY COMPARATORS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11520		74ACT11520		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
V _{OL}	I _{OL} = 50 µA	4.5 V			0.1	0.1		0.1		V
		5.5 V			0.1	0.1		0.1		
	I _{OL} = 24 mA	4.5 V			0.36	0.5		0.44		
		5.5 V			0.36	0.5		0.44		
	I _{OL} = 50 mA [†]	5.5 V				1.65				
I _{CC}	I _{OL} = 75 mA [†]	5.5 V						1.65		µA
	I _{IH}	V _I = V _{CC} , Q inputs only	5.5 V		10	10		10		
	I _{IL}	V _I = GND, Q inputs only	5.5 V		-0.3 -0.6	-1		-1		
	I _I	V _I = V _{CC} or GND, P and \overline{Q} inputs only	5.5 V		±0.1	±1		±1		
	Q inputs at GND		5.5 V		2.3 4.8	8		8		
ΔI _{CC} [‡]	Other inputs V _I = V _{CC} or GND		5.5 V							mA
	Q inputs open		5.5 V			160		80		
	Other inputs V _I = V _{CC} or GND		5.5 V							
C _i	Q inputs open		5.5 V		0.9	1		1		pF
	One input at 3.4 V and other inputs at V _{CC} or GND, P and \overline{Q} inputs only		5.5 V							
	V _I = V _{CC} or GND	5 V		3.5						

[†]Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡]This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

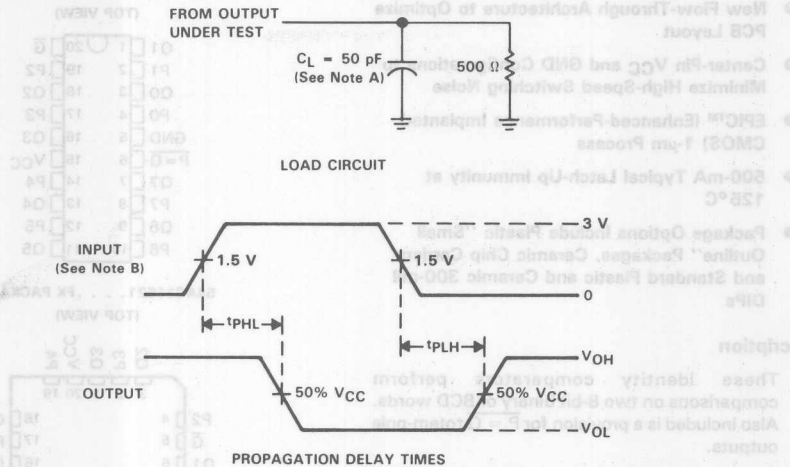
switching characteristics V_{CC} = 5 V ± 0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54ACT11520		74ACT11520		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	P or Q	$\overline{P} = \overline{Q}$	1.5	8.6	12.7	1.5	15.4	1.5	14.3	ns
t _{PHL}			1.5	8	12.4	1.5	14.8	1.5	13.9	
t _{PLH}	\overline{Q}	$\overline{P} = \overline{Q}$	1.5	6.4	8.5	1.5	10.2	1.5	9.5	ns
t _{PHL}			1.5	5.8	9	1.5	10.4	1.5	9.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	C _L = 50 pF, f = 1 MHz	40	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_0 = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

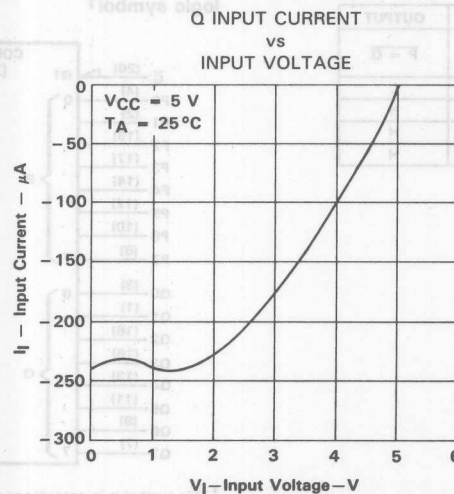


FIGURE 2

54AC11521, 74AC11521

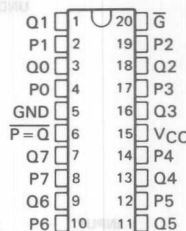
8-BIT IDENTITY COMPARATORS

D2957, JULY 1987—REVISED SEPTEMBER 1987

- Compares Two 8-Bit Words
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

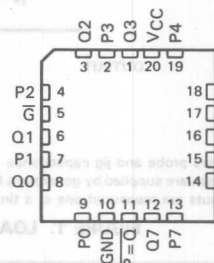
54AC11521 . . . J PACKAGE
74AC11521 . . . DW OR N PACKAGE

(TOP VIEW)



54AC11521 . . . FK PACKAGE

(TOP VIEW)



description

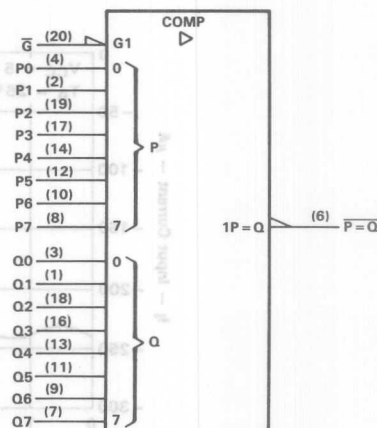
These identity comparators perform comparisons on two 8-bit binary or BCD words. Also included is a provision for $P = Q$ totem-pole outputs.

The 54AC11521 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74AC11521 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE G	$P = Q$
$P = Q$	L	L
$P > Q$	L	H
$P < Q$	L	H
X	H	H

logic symbol†



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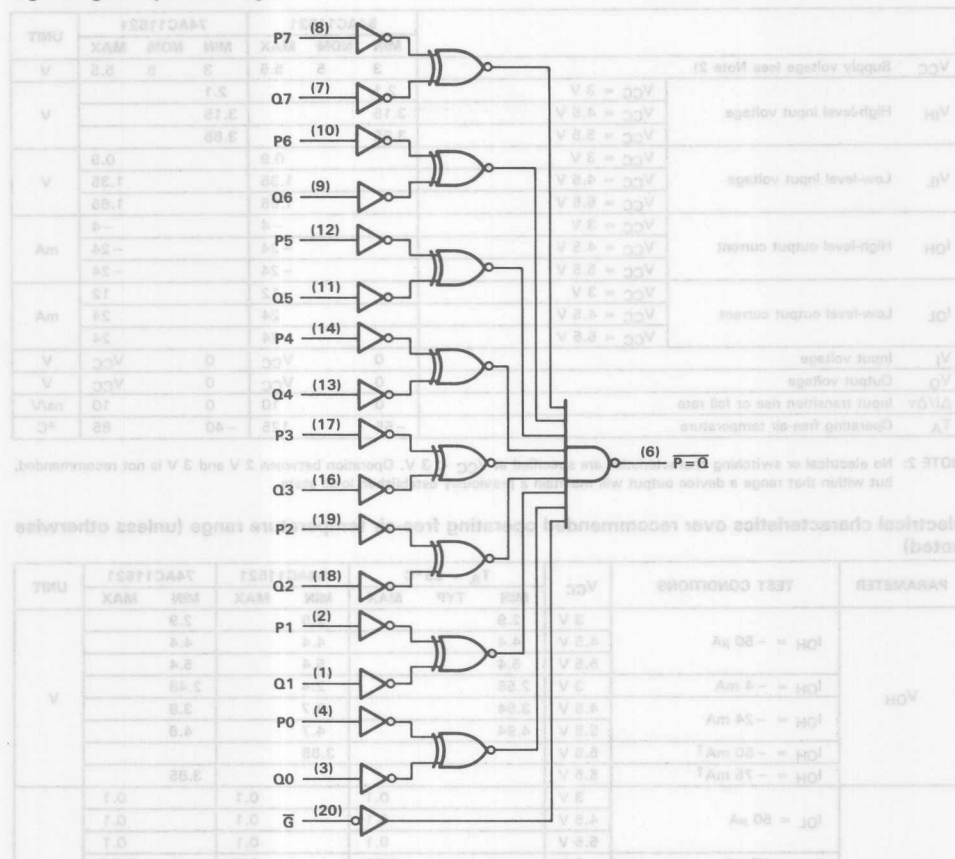
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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TEXAS
INSTRUMENTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54AC11521, 74AC11521
8-BIT IDENTITY COMPARATORS

recommended operating conditions

			54AC11521			74AC11521			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1			2.1			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 5.5 V	3.85			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V			0.9			0.9	V
		V _{CC} = 4.5 V			1.35			1.35	
		V _{CC} = 5.5 V			1.65			1.65	
I _{OH}	High-level output current	V _{CC} = 3 V			-4			-4	mA
		V _{CC} = 4.5 V			-24			-24	
		V _{CC} = 5.5 V			-24			-24	
I _{OL}	Low-level output current	V _{CC} = 3 V			12			12	mA
		V _{CC} = 4.5 V			24			24	
		V _{CC} = 5.5 V			24			24	
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise or fall rate		0		10	0		10	ns/V
T _A	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11521		74AC11521		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
	I _{OH} = -24 mA	5.5 V	4.94			4.7		4.8		
		5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
	I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	
		5.5 V				1.65			1.65	
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μA
C _i	V _I = V _{CC} or GND	5 V			4					pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

54AC11521, 74AC11521 8-BIT IDENTITY COMPARATORS

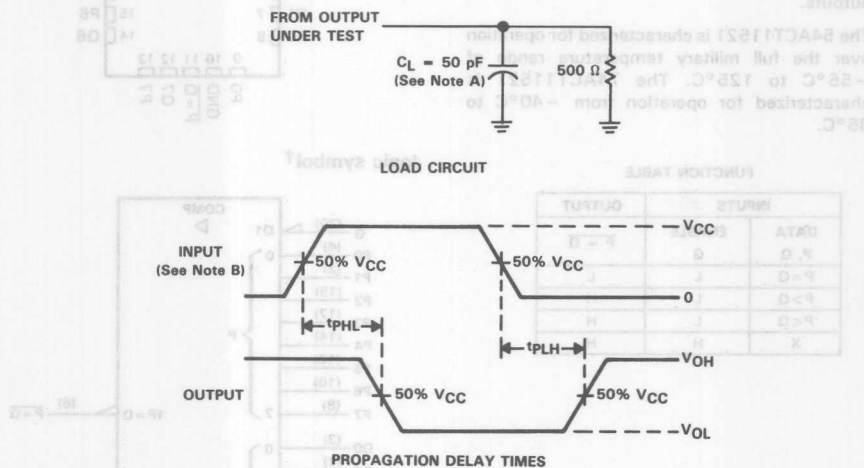
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			54AC11521		74AC11521		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	P or Q	$\overline{P} = \overline{Q}$	3.3 ± 0.3 V	1.5	12.5	16.6	1.5	20.4	1.5	19	ns
			5 ± 0.5 V	1.5	8.3	11.3	1.5	14	1.5	13	
t _{PHL}			3.3 ± 0.3 V	1.5	10.5	14.1	1.5	17.4	1.5	16.1	ns
			5 ± 0.5 V	1.5	7.2	10.1	1.5	12.2	1.5	11.4	
t _{PLH}	\overline{G}	$\overline{P} = \overline{Q}$	3.3 ± 0.3 V	1.5	7.1	9.8	1.5	11.4	1.5	10.8	ns
			5 ± 0.5 V	1.5	5.1	7.1	1.5	8.4	1.5	7.9	
t _{PHL}			3.3 ± 0.3 V	1.5	6.4	8.8	1.5	10.8	1.5	10.1	ns
			5 ± 0.5 V	1.5	4.8	7.1	1.5	8.6	1.5	8.1	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	C _L = 50 pF, f = 1 MHz	42	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54ACT11521, 74ACT11521 8-BIT IDENTITY COMPARATORS

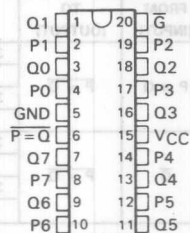
D2957, JULY 1987—REVISED SEPTEMBER 1987

- Compares Two 8-Bit Words
- Inputs are TTL-Voltage Compatible

54ACT11521 . . . J PACKAGE
74ACT11521 . . . DW OR N PACKAGE

(TOP VIEW)

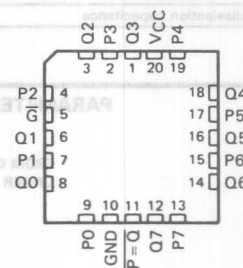
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPICTM (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C



- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54ACT11521 . . . FK PACKAGE

(TOP VIEW)



description

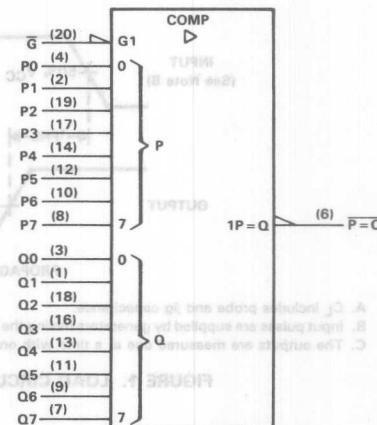
These identity comparators perform comparisons on two 8-bit binary or BCD words. Also included is a provision for $P = Q$ totem-pole outputs.

The 54ACT11521 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74ACT11521 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE G	$P = Q$
$P = Q$	L	L
$P > Q$	L	H
$P < Q$	L	H
X	H	H

logic symbol†



EPIC is a trademark of Texas Instruments Incorporated.

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

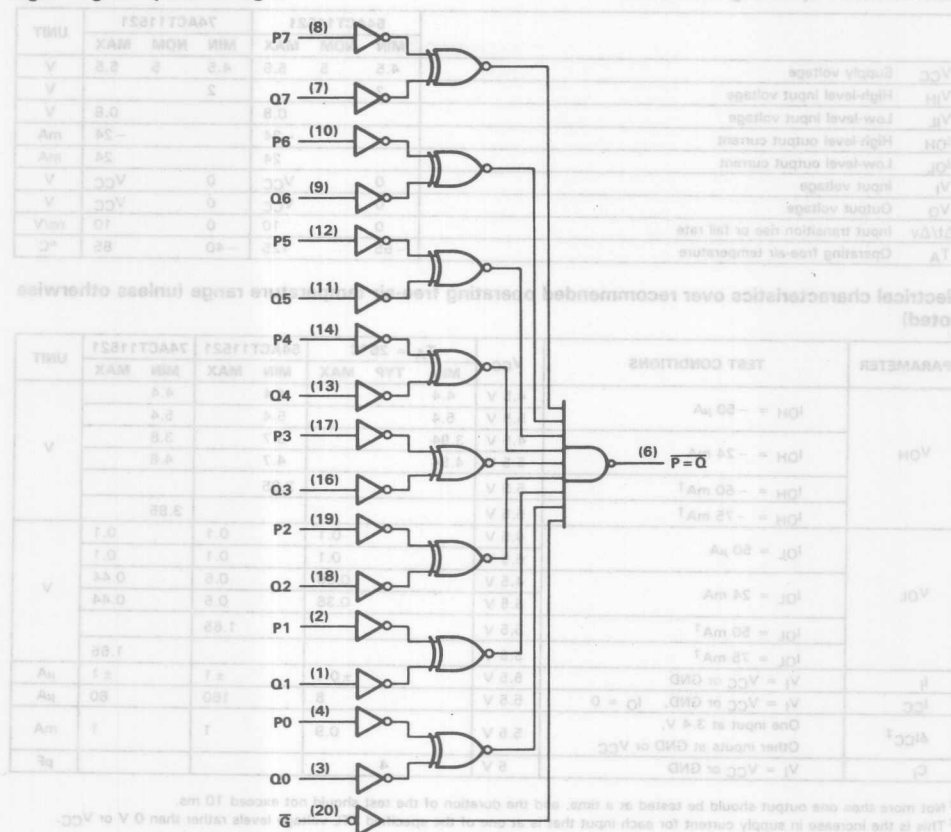
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54AC11521, 74AC11521 8-BIT IDENTITY COMPARATORS

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54ACT11521, 74ACT11521 8-BIT IDENTITY COMPARATORS

recommended operating conditions

		54ACT11521			74ACT11521			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-24			-24	mA
I _{OL}	Low-level output current			24			24	mA
V _I	Input voltage	0		V _{CC}	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise or fall rate	0		10	0		10	ns/V
T _A	Operating free-air temperature	-55		125	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11521		74ACT11521		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	4.5 V		0.1		0.1		0.1		V
		5.5 V		0.1		0.1		0.1		
	I _{OL} = 24 mA	4.5 V		0.36		0.5		0.44		
		5.5 V		0.36		0.5		0.44		
	I _{OL} = 50 mA [†]	5.5 V				1.65				
I _I	V _I = V _{CC} or GND	5.5 V		±0.1		±1		±1		μA
		5.5 V		8		160		80		
	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V		0.9		1		1		
		5.5 V								
	V _I = V _{CC} or GND	5 V		4						

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

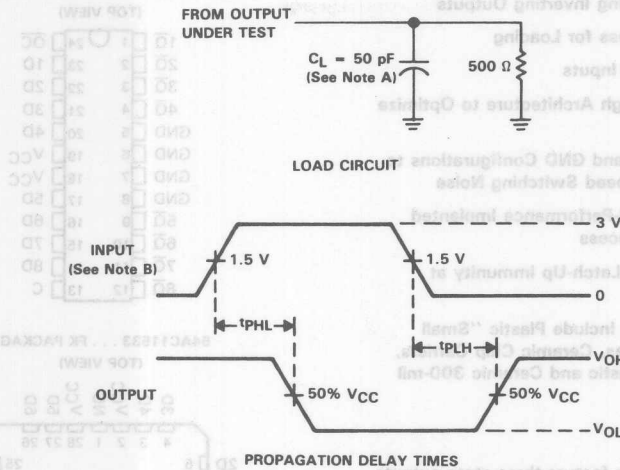
switching characteristics V_{CC} = 5 V ± 0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54ACT11521		74ACT11521		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	P or Q	P = Q	1.5	8.8	13	1.5	15.9	1.5	14.7	ns
t _{PHL}			1.5	8.2	12	1.5	14.6	1.5	13.6	
t _{PLH}	Q	P = Q	1.5	6.7	9.3	1.5	11.2	1.5	10.5	ns
t _{PHL}			1.5	6.8	8.8	1.5	10.2	1.5	9.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance C _L = 50 pF, f = 1 MHz	40	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_0 = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. The outputs are measured one at a time with one input transition per measurement.

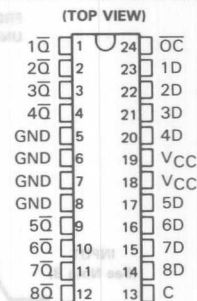
FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54AC11533, 74AC11533 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

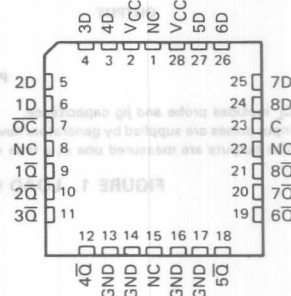
D2957, JULY 1987

- 8-Latches in a Single Package
- 3-State Bus-Driving Inverting Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54AC11533 . . . JT PACKAGE
74AC11533 . . . DW OR NT PACKAGE



54AC11533 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'AC11533 are transparent D-type latches. While the enable (C) is high, the \bar{Q} outputs will follow the complements of the (D) inputs. When the enable is taken low, the \bar{Q} outputs will be latched at the inverses of the levels that were set up at the D inputs. The 'AC11533 is functionally equivalent to the 'AC11373 except for having inverted outputs.

A buffered output-control (\bar{OC}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The 54AC11533 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74AC11533 is characterized for operation from 40°C to 85°C .

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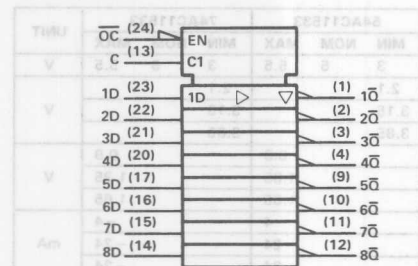
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54AC11533, 74AC11533 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

logic symbol†



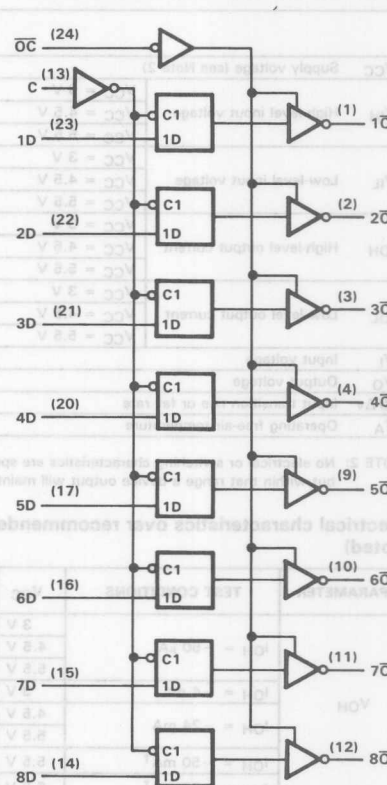
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
\overline{OC}	ENABLE C	D	\overline{Q}
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q_0}$
H	X	X	Z

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54AC11533, 74AC11533
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

			54AC11533			74AC11533			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3\text{ V}$			2.1			2.1	V
		$V_{CC} = 4.5\text{ V}$			3.15			3.15	
		$V_{CC} = 5.5\text{ V}$			3.85			3.85	
V_{IL}	Low-level input voltage	$V_{CC} = 3\text{ V}$						0.9	V
		$V_{CC} = 4.5\text{ V}$						1.35	
		$V_{CC} = 5.5\text{ V}$						1.65	
		$V_{CC} = 3\text{ V}$			-4			-4	
I_{OH}	High-level output current	$V_{CC} = 4.5\text{ V}$			-24			-24	mA
		$V_{CC} = 5.5\text{ V}$			-24			-24	
		$V_{CC} = 3\text{ V}$			12			12	
I_{OL}	Low-level output current	$V_{CC} = 4.5\text{ V}$			24			24	mA
		$V_{CC} = 5.5\text{ V}$			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: No electrical or switching characteristics are specified at $V_{CC} < 3\text{ V}$. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			54AC11533		74AC11533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50\text{ }\mu\text{A}$	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -4\text{ mA}$	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
	$I_{OH} = -24\text{ mA}$	5.5 V	4.94			4.7		4.8		
	$I_{OH} = -50\text{ mA}^\dagger$	5.5 V				3.85				
V_{OL}	$I_{OH} = -75\text{ mA}^\dagger$	5.5 V						3.85		V
	$I_{OL} = 50\text{ }\mu\text{A}$	3 V			0.1	0.1		0.1		
		4.5 V			0.1	0.1		0.1		
		5.5 V			0.1	0.1		0.1		
	$I_{OL} = 12\text{ mA}$	3 V			0.36	0.5		0.44		
	$I_{OL} = 24\text{ mA}$	4.5 V			0.36	0.5		0.44		
	$I_{OL} = 24\text{ mA}$	5.5 V			0.36	0.5		0.44		
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			± 0.5	± 10		± 5		μA
	$V_I = V_{CC}$ or GND	5.5 V			± 0.1	± 1		± 1		
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8	160		80		μA
C_i	$V_I = V_{CC}$ or GND	5 V			4					pF
C_o	$V_O = V_{CC}$ or GND	5.5 V			10					pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

2

Advanced CMOS Circuits

54AC11533, 74AC11533
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

timing requirements (see Figure 1)

		V _{CC} RANGE	T _A = 25°C		54AC11533		74AC11533		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, enable C high	3.3 ± 0.3 V	5.5		5.5		5.5		ns
		5 ± 0.5 V	4		4		4		
t _{su}	Setup time, data before enable C↓	3.3 ± 0.3 V	4		4		4		ns
		5 ± 0.5 V	3.5		3.5		3.5		
t _h	Hold time, data after enable C↓	3.3 ± 0.3 V	2		2		2		ns
		5 ± 0.5 V	2		2		2		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C			54AC11533		74AC11533		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	\bar{Q}	3.3 ± 0.3 V	1.5	8.5	12.6	1.5	15.2	1.5	14.3	ns
			5 ± 0.5 V	1.5	5.5	8.4	1.5	10.6	1.5	9.8	
t _{PHL}			3.3 ± 0.3 V	1.5	7.5	10.1	1.5	12	1.5	11.3	
			5 ± 0.5 V	1.5	5	7.1	1.5	8.6	1.5	8	
t _{PLH}	C	Any \bar{Q}	3.3 ± 0.3 V	1.5	10	14.5	1.5	17.6	1.5	16.5	ns
			5 ± 0.5 V	1.5	6.5	10	1.5	12.1	1.5	11.3	
t _{PHL}			3.3 ± 0.3 V	1.5	9.5	12.8	1.5	15.2	1.5	14.3	
			5 ± 0.5 V	1.5	6.5	9.1	1.5	11	1.5	10.3	
t _{PZH}	\bar{OC}	Any \bar{Q}	3.3 ± 0.3 V	1.5	9	13.1	1.5	15.7	1.5	14.7	ns
			5 ± 0.5 V	1.5	6.5	9.5	1.5	11.7	1.5	10.8	
t _{PZL}			3.3 ± 0.3 V	1.5	8.5	11.6	1.5	14.1	1.5	13.1	
			5 ± 0.5 V	1.5	6	8.6	1.5	10.9	1.5	9.7	
t _{PHZ}	\bar{OC}	Any \bar{Q}	3.3 ± 0.3 V	1.5	9.5	12	1.5	13.2	1.5	12.8	ns
			5 ± 0.5 V	1.5	8.5	10.7	1.5	11.7	1.5	11.4	
t _{PLZ}			3.3 ± 0.3 V	1.5	7.5	10.2	1.5	11.4	1.5	11	
			5 ± 0.5 V	1.5	6	8.2	1.5	9.3	1.5	8.9	

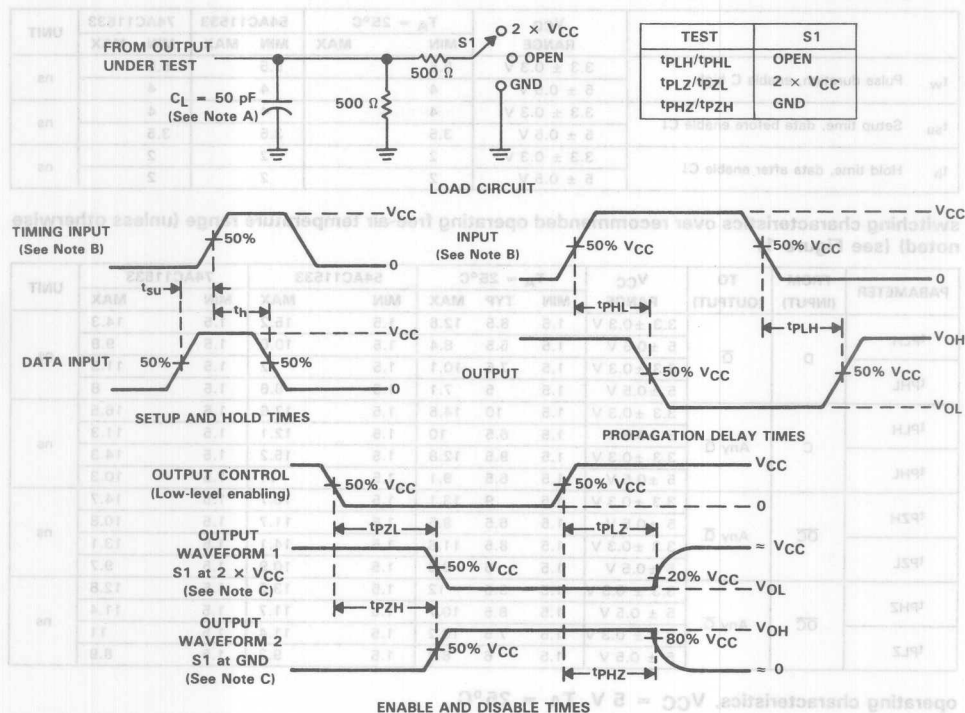
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per latch	Outputs enabled	C _L = 50 pF, f = 1 MHz	55	pF
		Outputs disabled		44	

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54AC11533, 74AC11533
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54ACT11533, 74ACT11533 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

D2957, JULY 1987

- 8-Latches in a Single Package
- 3-State Bus-Driving Inverting Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'ACT11533 are transparent D-type latches. While the enable (C) is high, the \bar{Q} outputs will follow the complements of the (D) inputs. When the enable is taken low, the \bar{Q} outputs will be latched at the inverses of the levels that were set up at the D inputs. The 'ACT11533 is functionally equivalent to the 'ACT11373 except for having inverted outputs.

A buffered output-control (\bar{OC}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The 54ACT11533 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11533 is characterized for operation from -40°C to 85°C.

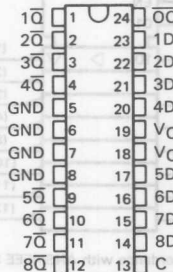
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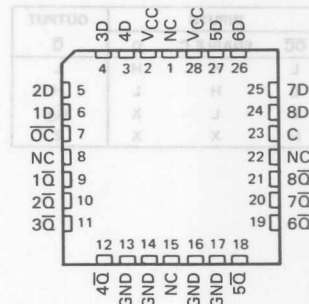
54ACT11533 ... JT PACKAGE
74ACT11533 ... DW OR NT PACKAGE

(TOP VIEW)



54ACT11533 ... FK PACKAGE

(TOP VIEW)



NC—No internal connection

2

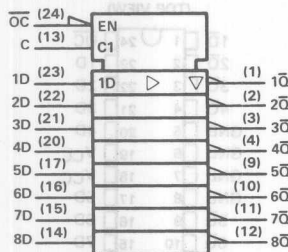
Advanced CMOS Circuits

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54ACT11533, 74ACT11533 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

logic symbol†



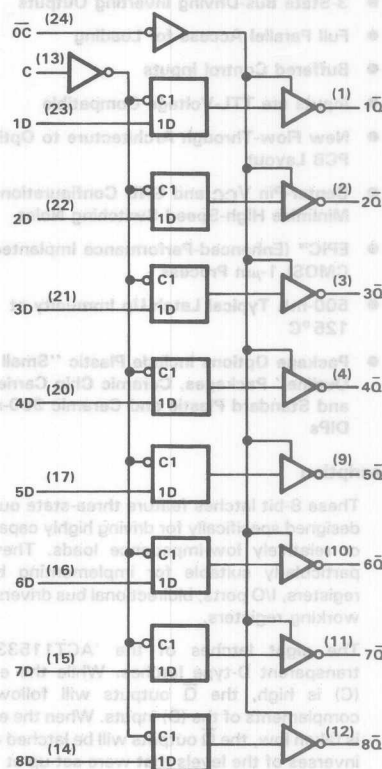
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
OC	ENABLE C	D	Q
L	H	H	L
L	H	L	H
L	L	X	Q _O
H	X	X	Z

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC}	-0.5 V to 7 V
Input voltage, V _I (see Note 1)	-0.5 V to V _{CC} + 0.5 V
Output voltage, V _O (see Note 1)	-0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND pins	±200 mA
Storage temperature range	-65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54ACT11533, 74ACT11533
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	TEST CONDITIONS	54ACT11533		74ACT11533		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		-24		-24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			54ACT11533		74ACT11533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	$I_{OH} = -50 \text{ mA}^\dagger$	5.5 V				3.85				
V_{OL}	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1	0.1		0.1		V
		5.5 V			0.1	0.1		0.1		
	$I_{OL} = 24 \text{ mA}$	4.5 V			0.36	0.5		0.44		
		5.5 V			0.36	0.5		0.44		
	$I_{OL} = 50 \text{ mA}^\dagger$	5.5 V				1.65				
I_{OZ}	$V_O = V_{CC} \text{ or GND}$	5.5 V			± 0.5	± 10		± 5		μA
		5.5 V			± 0.1	± 1		± 1		
	$V_I = V_{CC} \text{ or GND, } I_O = 0$	5.5 V			8	160		80		
		5.5 V			0.9	1		1		
	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V								
ΔI_{CC}^\ddagger		5.5 V								mA
C_i	$V_I = V_{CC} \text{ or GND}$	5 V			4					pF
C_o	$V_O = V_{CC} \text{ or GND}$	5 V			10					pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

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Advanced CMOS Circuits

54ACT11533, 74ACT11533 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

timing requirements, $V_{CC} = 5 \pm 0.5 \text{ V}$ (see Figure 1)

PARAMETER	DESCRIPTION	$T_A = 25^\circ\text{C}$		54ACT11533		74ACT11533		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, enable C high	5		5		5		ns
t_{su}	Setup time, data before enable C↓	3.5		3.5		3.5		ns
t_h	Hold time data after enable C↓	3.5		3.5		3.5		ns

switching characteristics, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (see Figure 1)

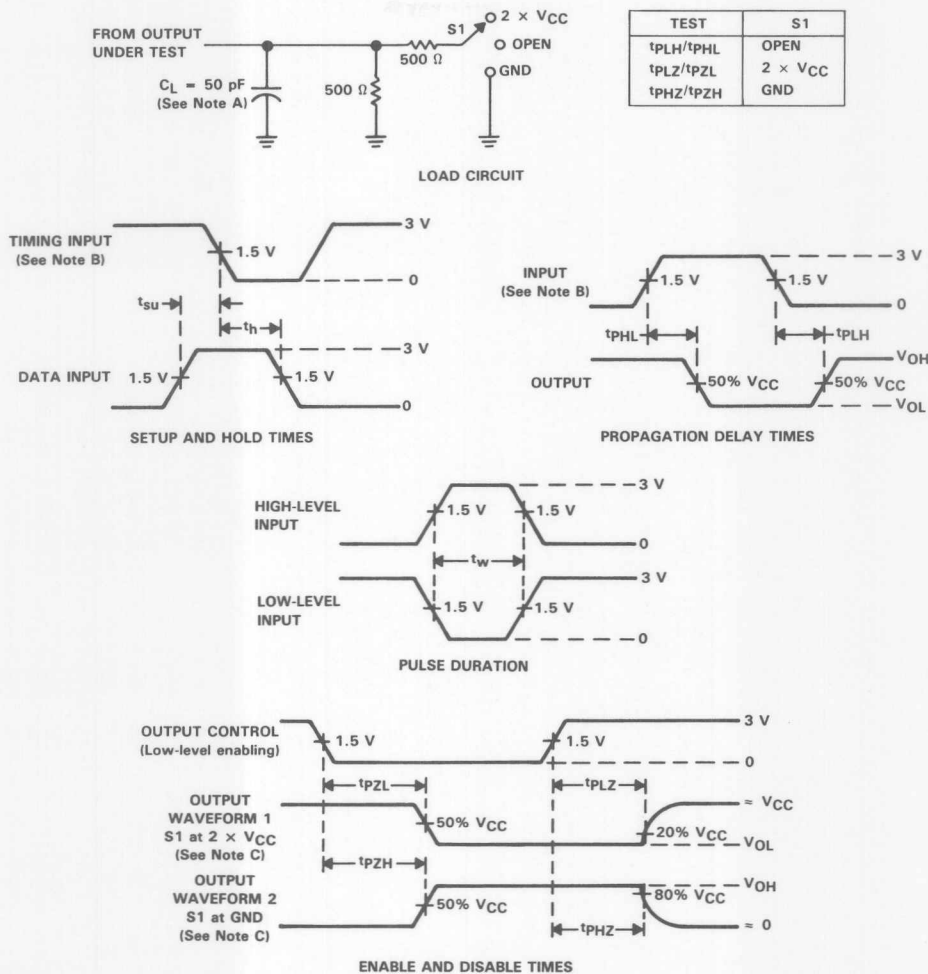
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11533		74ACT11533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	\bar{Q}	1.5	7	10.1	1.5	11.9	1.5	11.3	ns
t_{PHL}	D	\bar{Q}	1.5	6.5	8.4	1.5	10.2	1.5	9.5	
t_{PLH}	C	Any Q	1.5	8.5	11.3	1.5	14.1	1.5	13	ns
t_{PHL}	C	Any Q	1.5	8.5	10.7	1.5	13.2	1.5	12.2	
t_{PZH}	\bar{OC}	Any Q	1.5	7.5	10.7	1.5	13.6	1.5	12.5	ns
t_{PZL}	\bar{OC}	Any Q	1.5	7.5	10.9	1.5	12.9	1.5	12	
t_{PHZ}	\bar{OC}	Any Q	1.5	10.5	12.1	1.5	13.1	1.5	12.8	ns
t_{PLZ}	\bar{OC}	Any Q	1.5	7.5	9.5	1.5	10.7	1.5	10.3	

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	DESCRIPTION	TEST CONDITIONS		TYP	UNIT
		Outputs enabled	Outputs disabled		
C_{pd}	Power dissipation capacitance per latch	$C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$		69	pF
				58	

54ACT11533, 74ACT11533 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION

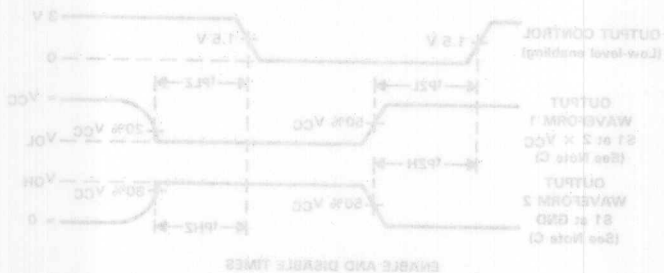
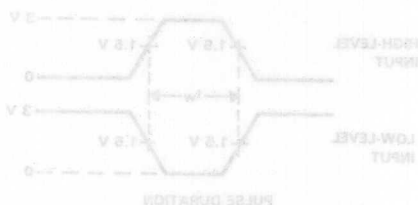
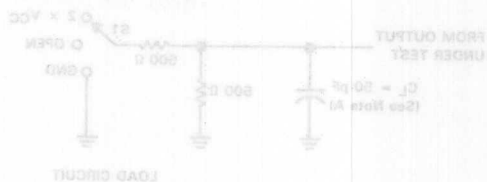


- NOTES: A. C_L includes probe and jig capacitance.
 B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_0 = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION

TEST	TEST
WAVEFORM 1	WAVEFORM 2
WAVEFORM 3	WAVEFORM 4
WAVEFORM 5	WAVEFORM 6



NOTES: A. CL includes probe and jig capacitance.
 B. Input pulses are supplied by generator having the following characteristics: PRR ≤ 10 MHz, $t_r = 50$ ns, $t_f = 5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54AC11534, 74AC11534 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2957, JULY 1987

- 8 D-Type Flip-Flops in a Single Package
- High-Current 3-State True Outputs Can Drive Up to 15 LSTTL Loads
- Full Parallel Access for Loading
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ACT11534 are edge-triggered D-type flip-flops. On the positive transition of the clock, the \bar{Q} outputs will be set to the logic levels that were set up at the D inputs. The ACT11534 is functionally equivalent to the ACT11374 except for having inverted outputs.

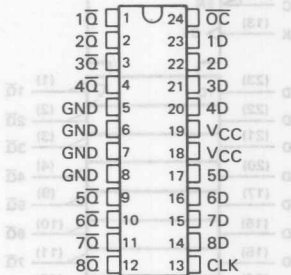
An output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control (\bar{OC}) does not affect the internal operation of the flip-flops. Old data can be retained, or new data can be entered while the outputs are in the high-impedance state.

The 54ACT11534 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74ACT11534 is characterized for operation from -40°C to 85°C .

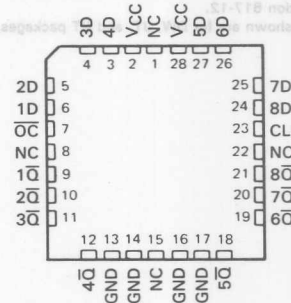
54AC11534 ... JT PACKAGE
74AC11534 ... DW OR NT PACKAGE

(TOP VIEW)



54AC11534 ... FK PACKAGE

(TOP VIEW)



NC—No internal connection

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\bar{OC}	CLK	D	\bar{Q}
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

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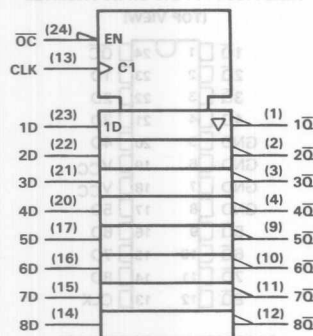
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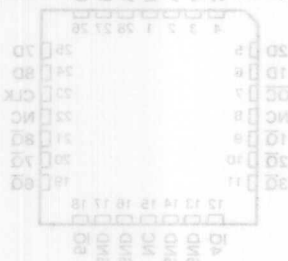
2-195

54AC11534, 74AC11534 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

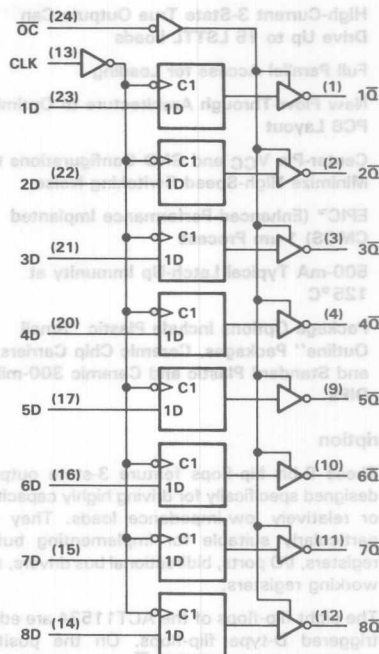
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.



logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

The 54AC11534 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC11534 is characterized for operation from -40°C to 85°C.

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Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11534, 74AC11534
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	TEST CONDITIONS	V _{CC}	54AC11534			74AC11534			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1			2.1			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 5.5 V	3.85			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V			0.9			0.9	V
		V _{CC} = 4.5 V			1.35			1.35	
		V _{CC} = 5.5 V			1.65			1.65	
I _{OH}	High-level output current	V _{CC} = 3 V			-4			-4	mA
		V _{CC} = 4.5 V			-24			-24	
		V _{CC} = 5.5 V			-24			-24	
I _{OL}	Low-level output current	V _{CC} = 3 V			12			12	mA
		V _{CC} = 4.5 V			24			24	
		V _{CC} = 5.5 V			24			24	
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise or fall rate		0		10	0		10	ns/V
T _A	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11534		74AC11534		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
V _{OL}	I _{OH} = -50 mA [†]	5.5 V				3.85				V
		5.5 V						3.85		
		5.5 V								
	I _{OL} = 50 μA	3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA [†]	5.5 V				1.65				
		5.5 V						1.65		
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5	±10		±5		μA
I _I	V _I = V _{CC} or GND	5.5 V			±0.1	±1		±1		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8	160		80		μA
C _i	V _I = V _{CC} or GND	5 V		4						pF
C _o	V _O = V _{CC} or GND	5 V		10						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

54AC11534, 74AC11534 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

timing requirements (see Figure 1)

TIME			VCC RANGE	TA = 25°C		54AC11534		74AC11534		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		3.3 ± 0.3 V	0	100	0	100	0	100	MHz
			5 ± 0.5 V	0	125	0	125	0	125	
t _w	Pulse duration	CLK low or	3.3 ± 0.3 V	4		4		4		ns
		CLK high	5 ± 0.5 V	4		4		4		
t _{su}	Setup time, data before CLK↑		3.3 ± 0.3 V	5		5		5		ns
			5 ± 0.5 V	4		4		4		
t _h	Hold time, data after CLK↑		3.3 ± 0.3 V	5		5		5		ns
			5 ± 0.5 V	3.5		3.5		3.5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC RANGE	TA = 25°C			54AC11534		74AC11534		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	CLK	Any Q	3.3 ± 0.3 V								ns
			5 ± 0.5 V		7.1						
t _{PHL}			3.3 ± 0.3 V								
			5 ± 0.5 V		7.1						
t _{PZH}	\overline{OC}	Any Q	3.3 ± 0.3 V								ns
			5 ± 0.5 V		6.6						
t _{PZL}			3.3 ± 0.3 V								
			5 ± 0.5 V		6.2						
t _{PHZ}	\overline{OC}	Any Q	3.3 ± 0.3 V								ns
			5 ± 0.5 V		7.2						
t _{PLZ}			3.3 ± 0.3 V								
			5 ± 0.5 V		7.1						

operating characteristics, VCC = 5 V, TA = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C _L = 50 pF, f = 1 MHz		75	pF
		Outputs disabled			65	

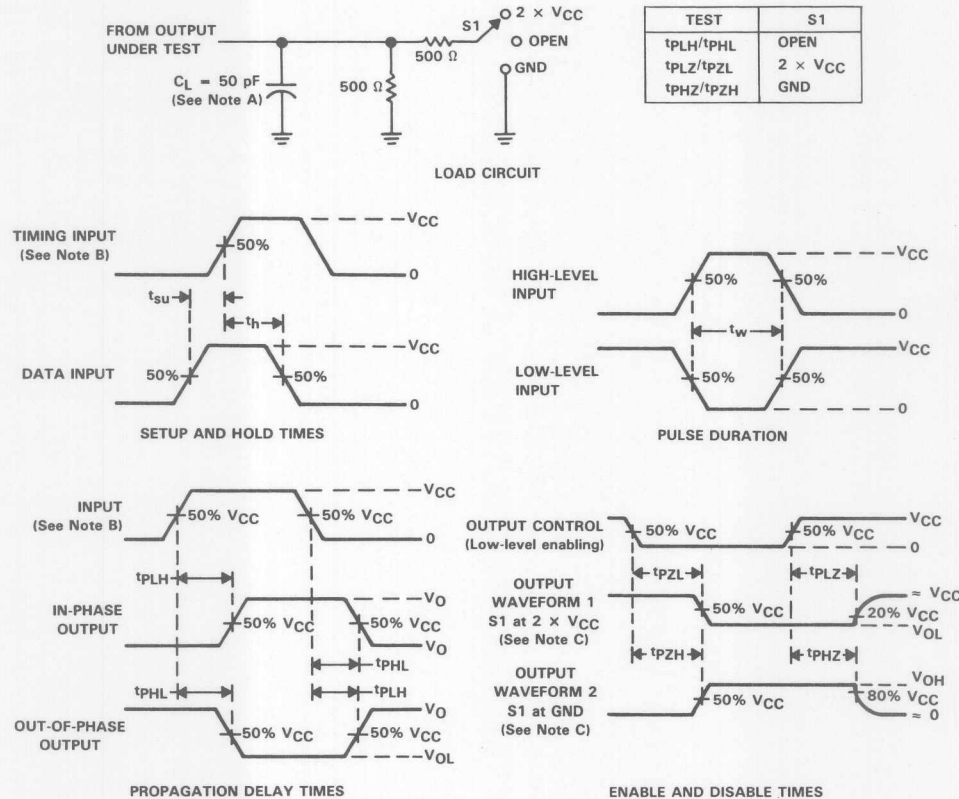
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Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11534, 74AC11534
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 For testing f_{max} and pulse duration: $t_r = 1$ to 3 ns , $t_f = 1$ to 3 ns .

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54ACT11534, 74ACT11534 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2957, JULY 1987

- 8 D-Type Flip-Flops in a Single Package
- High-Current 3-State True Outputs Can Drive Up to 15 LSTTL Loads
- Full Parallel Access for Loading
- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ACT11534 are edge-triggered D-type flip-flops. On the positive transition of the clock, the \bar{Q} outputs will be set to the logic levels that were set up at the D inputs. The ACT11534 is functionally equivalent to the ACT11374 except for having inverted outputs.

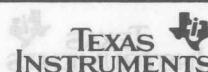
An output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control (\bar{OC}) does not affect the internal operation of the flip-flops. Old data can be retained, or new data can be entered while the outputs are in the high-impedance state.

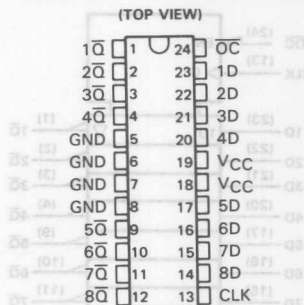
The 54ACT11534 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11534 is characterized for operation from -40°C to 85°C.

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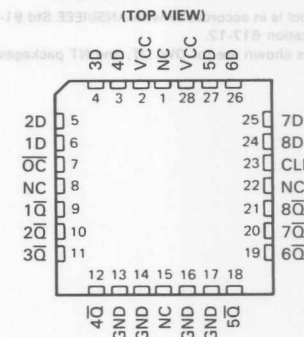
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54ACT11534 ... JT PACKAGE
74ACT11534 ... DW OR NT PACKAGE



54ACT11534 ... FK PACKAGE



NC—No internal connection

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\bar{OC}	CLK	D	\bar{Q}
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

2

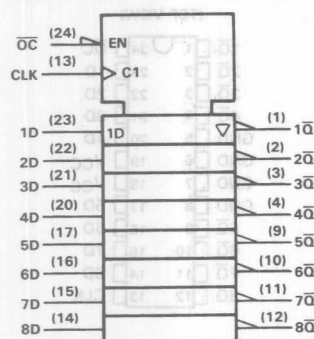
Advanced CMOS Circuits

PRODUCT PREVIEW

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54ACT11534, 74ACT11534 **OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS** **WITH 3-STATE OUTPUTS**

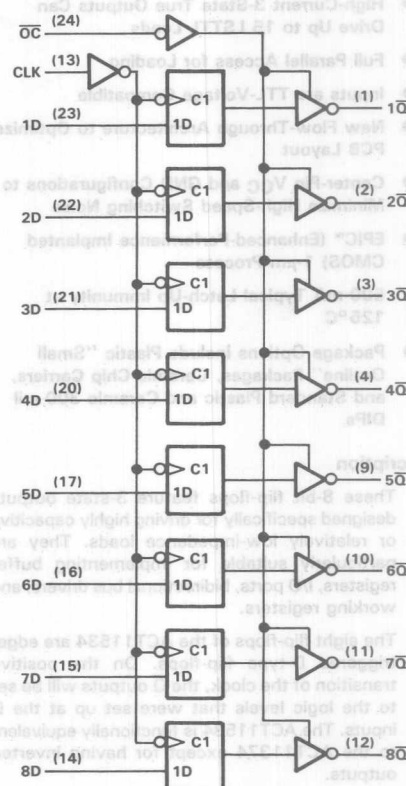
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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Advanced CMOS Circuits

PRODUCT PREVIEW

54ACT11534, 74ACT11534
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C		54ACT11534		74ACT11534		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	
V _{CC}	Supply voltage		4.5	5.5		4.5	5.5		V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage			0.8			0.8		V
I _{OH}	High-level output current				-24		-24		mA
I _{OL}	Low-level output current				24		24		mA
V _I	Input voltage		0	V _{CC}		0	V _{CC}		V
V _O	Output voltage		0	V _{CC}		0	V _{CC}		V
Δt/Δv	Input transition rise or fall rate		0	10		0	10		ns/V
T _A	Operating free-air temperature		-55	125		-40	85		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11534		74ACT11534		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA [†]	5.5 V				1.65				
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±10		±5	μA
		5.5 V			±0.1		±1		±1	
	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	
		5.5 V			0.9		1		1	
	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.9		1		1	
C _i	V _I = V _{CC} or GND	5 V		4						pF
C _o	V _O = V _{CC} or GND	5 V		10						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements, V_{CC} = 5 ± 0.5 V (see Figure 1)

PARAMETER	TEST CONDITIONS	T _A = 25°C		54ACT11534		74ACT11534		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, enable C high							ns
t _{su}	Setup time, data before enable C ↓							ns
t _h	Hold time, data after enable C ↓							ns

54ACT11534, 74ACT11534 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see Figure 1)

PARAMETER	FROM	TO	T _A = 25°C			54ACT11534		74ACT11534		UNIT
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	CLK	Any Q	9.4							ns
t _{PHL}			9.5							
t _{PZH}	OC	Any Q	8.4							ns
t _{PZL}			8.1							
t _{PHZ}	OC	Any Q	8.3							ns
t _{PLZ}			9.2							

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	92	pF
		Outputs disabled		82	

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Advanced CMOS Circuits

PRODUCT PREVIEW

UNIT	54ACT11534		74ACT11534		$T_A = 25^\circ\text{C}$		V_{CC}		TEST CONDITIONS	PARAMETER
	MIN	MAX	MIN	MAX	MIN	TYP	MIN	MAX		
V	4.5		4.5		4.5		4.5		$I_{OH} = -30\text{ mA}$	V_{OH}
	4.2		4.2		4.2		4.2		$I_{OH} = -24\text{ mA}$	
	3.7		3.7		3.7		3.7		$I_{OH} = -20\text{ mA}$	
	4.1		4.1		4.1		4.1		$I_{OH} = -15\text{ mA}$	
	3.8		3.8		3.8		3.8		$I_{OH} = -10\text{ mA}$	
	3.8		3.8		3.8		3.8		$I_{OH} = -5\text{ mA}$	
V	0.1		0.1		0.1		0.1		$I_{OL} = 30\text{ mA}$	V_{OL}
	0.1		0.1		0.1		0.1		$I_{OL} = 24\text{ mA}$	
	0.05		0.05		0.05		0.05		$I_{OL} = 20\text{ mA}$	
	0.05		0.05		0.05		0.05		$I_{OL} = 15\text{ mA}$	
	0.05		0.05		0.05		0.05		$I_{OL} = 10\text{ mA}$	
	0.05		0.05		0.05		0.05		$I_{OL} = 5\text{ mA}$	
A_{OH}	2		2		2		2		$V_O = V_{CC}$ or GND	I_{OS}
A_{OL}	2		2		2		2		$V_I = V_{CC}$ or GND	I_I
A_{CC}	100		100		100		100		$V_I = V_{CC}$ or GND, $I_O = 0$	I_{CC}
A_{m}	1		1		0.9		0.9		One input at 3.4 V, other inputs at GND or V_{CC}	ΔI_{CC}^T
R_C					5		5		$V_I = V_{CC}$ or GND	C_I
R_Q					10		10		$V_O = V_{CC}$ or GND	C_Q

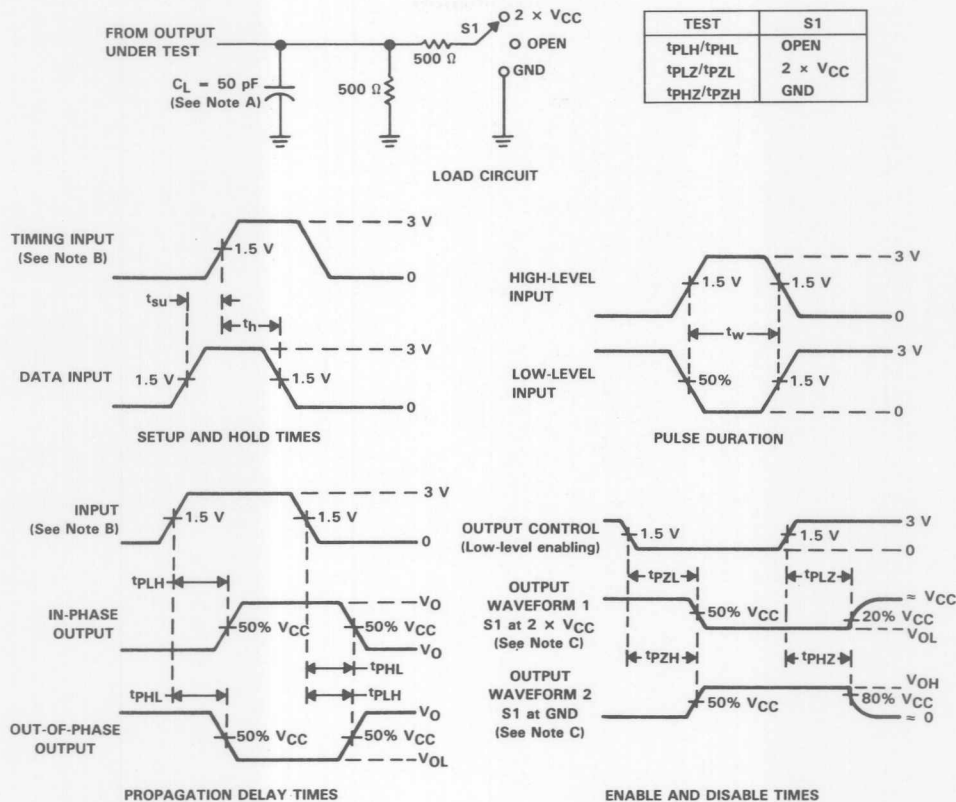
¹ Not more than one output should be loaded at a time, and the duration of the test should not exceed 10 ms.
² This is the increase in supply current for each input that is one of the specified TTL voltage levels rather than 0 V or V_{CC} .

Timing requirements, $V_{CC} = 5 \pm 0.5\text{ V}$ (see Figure 1)

UNIT	54ACT11534		74ACT11534		$T_A = 25^\circ\text{C}$	
	MIN	MAX	MIN	MAX	MIN	MAX
t_{w}						
t_{SU}						
t_{H}						

54ACT11534, 74ACT11534
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



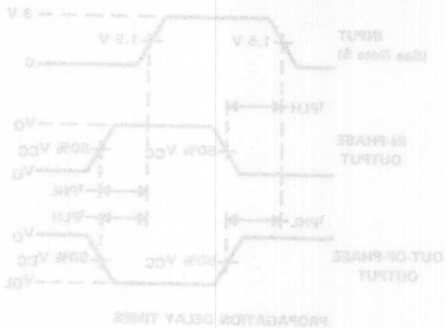
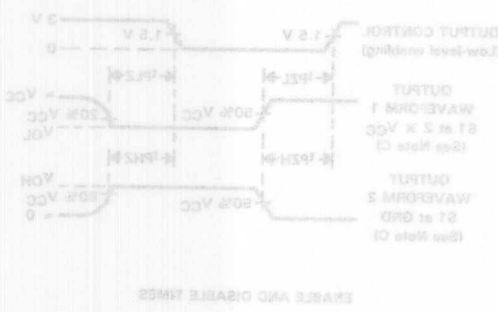
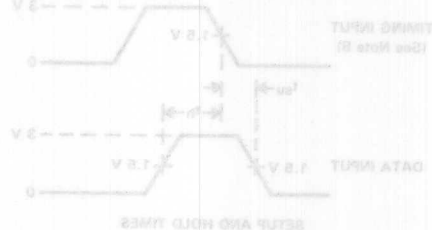
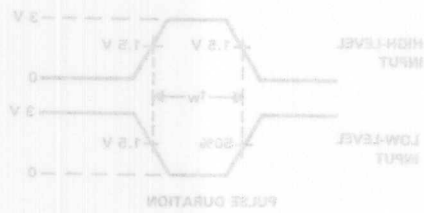
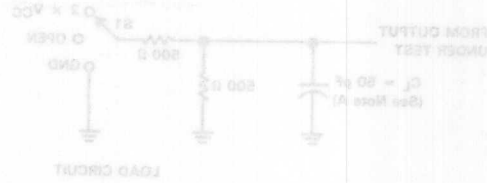
- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
For testing f_{max} and pulse duration: $t_r = 1 \text{ to } 3 \text{ ns}$, $t_f = 1 \text{ to } 3 \text{ ns}$.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

OCAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION

TEST	SI
DRIVE	DRIVE
3 X VCC	3 X VCC
GND	GND



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are applied by generators having the following characteristics: PRR ≤ 10 MHz, $t_r \leq 50$ ns, $t_f \leq 3$ ns.
C. Waveform 1 is for an input with internal conditions such that the output is low except when disabled by the output control.
D. The output is measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54AC11620, 74AC11620 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2957, JULY 1987

- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

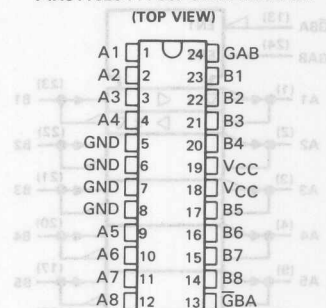
These devices allow data transmission from the A bus to the B bus, or from the B bus to the A bus, depending upon the logic levels at the enable inputs (GBA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

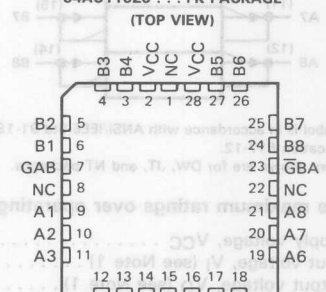
The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of GBA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be complementary for the AC11620.

The 54AC11620 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC11620 is characterized for operation from -40°C to 85°C.

54AC11620 . . . JT PACKAGE
74AC11620 . . . DW OR NT PACKAGE



54AC11620 . . . FK PACKAGE



NC—No internal connection

FUNCTION TABLE

ENABLE INPUTS		OPERATION
GBA	GAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus

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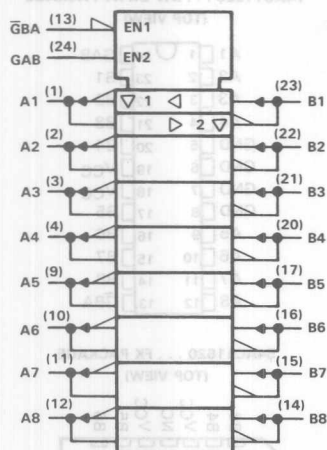
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Advanced CMOS Circuits

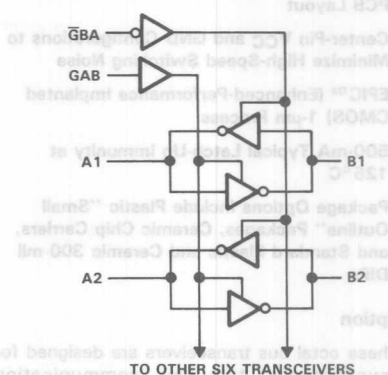
PRODUCT PREVIEW

54AC11620, 74AC11620 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

logic symbol†



logic diagram (positive logic)



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Advanced CMOS Circuits

PRODUCT PREVIEW

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

A data to B bus	H	H
B data to A bus	L	H
A data to B bus	H	L
B data to A bus	L	L

54AC11620, 74AC11620 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

			54AC11620			74AC11620			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1			2.1			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 5.5 V	3.85			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V			0.9			0.9	V
		V _{CC} = 4.5 V			1.35			1.35	
		V _{CC} = 5.5 V			1.65			1.65	
I _{OH}	High-level output current	V _{CC} = 3 V			-4			-4	mA
		V _{CC} = 4.5 V			-24			-24	
		V _{CC} = 5.5 V			-24			-24	
I _{OL}	Low-level output current	V _{CC} = 3 V			12			12	mA
		V _{CC} = 4.5 V			24			24	
		V _{CC} = 5.5 V			24			24	
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise or fall rate		0		10	0		10	ns/V
T _A	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11620		74AC11620		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA [†]	5.5 V				1.65				
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±10		±5	μA
	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μA
C _i	V _I = V _{CC} or GND	5 V		4						pF
C _o	V _O = V _{CC} or GND	5 V		10						pF

[†]Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

54AC11620, 74AC11620 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

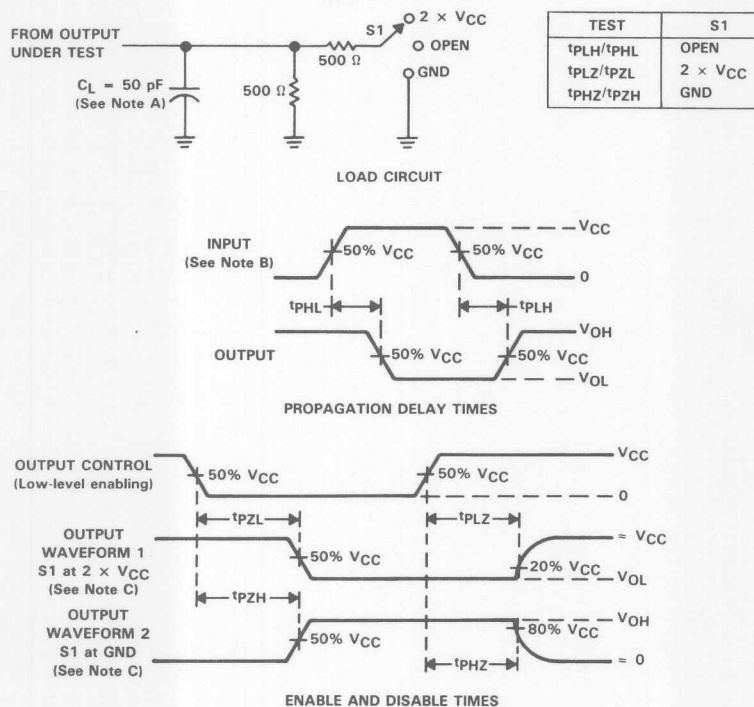
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C			54AC11620		74AC11620		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		4.3						
t _{PHL}	A or B	B or A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		4.8						
t _{PZH}	$\overline{\text{G}}$ BA	A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		4.5						
t _{PZL}	$\overline{\text{G}}$ BA	A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.1						
t _{PHZ}	$\overline{\text{G}}$ BA	A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.6						
t _{PLZ}	$\overline{\text{G}}$ BA	A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		4.2						
t _{PZH}	GAB	B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		4.9						
t _{PZL}	GAB	B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.6						
t _{PHZ}	GAB	B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.5						
t _{PLZ}	GAB	B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.6						

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per transceiver	45	pF
	Outputs enabled	12	pF
	Outputs disabled		
	C _L = 50 pF, f = 1 MHz		

54AC11620, 74AC11620 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION

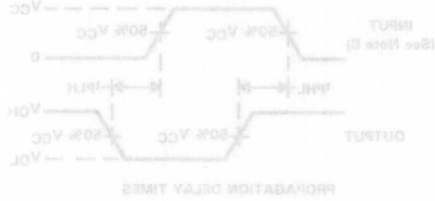
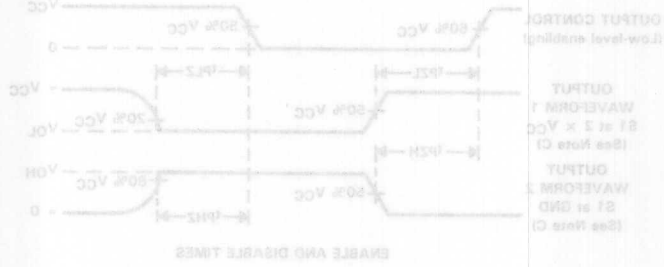


- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

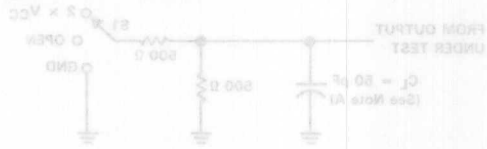
FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $V_L = 50$ V, $V_H = 50$ V, $t_r = 3$ ns, $t_f = 3$ ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.



LOAD CIRCUIT



TEST	TEST
WAVEFORM 1	WAVEFORM 2
WAVEFORM 3	WAVEFORM 4
WAVEFORM 5	WAVEFORM 6
WAVEFORM 7	WAVEFORM 8
WAVEFORM 9	WAVEFORM 10
WAVEFORM 11	WAVEFORM 12
WAVEFORM 13	WAVEFORM 14
WAVEFORM 15	WAVEFORM 16
WAVEFORM 17	WAVEFORM 18
WAVEFORM 19	WAVEFORM 20
WAVEFORM 21	WAVEFORM 22
WAVEFORM 23	WAVEFORM 24
WAVEFORM 25	WAVEFORM 26
WAVEFORM 27	WAVEFORM 28
WAVEFORM 29	WAVEFORM 30
WAVEFORM 31	WAVEFORM 32
WAVEFORM 33	WAVEFORM 34
WAVEFORM 35	WAVEFORM 36
WAVEFORM 37	WAVEFORM 38
WAVEFORM 39	WAVEFORM 40
WAVEFORM 41	WAVEFORM 42
WAVEFORM 43	WAVEFORM 44
WAVEFORM 45	WAVEFORM 46
WAVEFORM 47	WAVEFORM 48
WAVEFORM 49	WAVEFORM 50
WAVEFORM 51	WAVEFORM 52
WAVEFORM 53	WAVEFORM 54
WAVEFORM 55	WAVEFORM 56
WAVEFORM 57	WAVEFORM 58
WAVEFORM 59	WAVEFORM 60
WAVEFORM 61	WAVEFORM 62
WAVEFORM 63	WAVEFORM 64
WAVEFORM 65	WAVEFORM 66
WAVEFORM 67	WAVEFORM 68
WAVEFORM 69	WAVEFORM 70
WAVEFORM 71	WAVEFORM 72
WAVEFORM 73	WAVEFORM 74
WAVEFORM 75	WAVEFORM 76
WAVEFORM 77	WAVEFORM 78
WAVEFORM 79	WAVEFORM 80
WAVEFORM 81	WAVEFORM 82
WAVEFORM 83	WAVEFORM 84
WAVEFORM 85	WAVEFORM 86
WAVEFORM 87	WAVEFORM 88
WAVEFORM 89	WAVEFORM 90
WAVEFORM 91	WAVEFORM 92
WAVEFORM 93	WAVEFORM 94
WAVEFORM 95	WAVEFORM 96
WAVEFORM 97	WAVEFORM 98
WAVEFORM 99	WAVEFORM 100

PARAMETER MEASUREMENT INFORMATION

54ACT11620, 74ACT11620 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2957, JULY 1987

- Local Bus-Latch Capability
- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

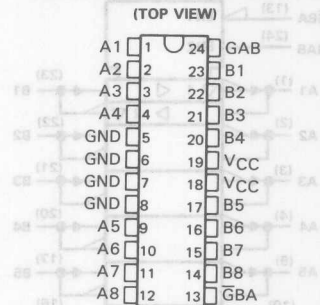
These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs (GBA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

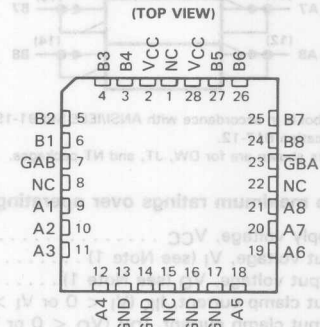
The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of GBA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be complementary for the ACT11620.

The 54ACT11620 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11620 is characterized for operation from -40°C to 85°C.

54ACT11620 . . . JT PACKAGE
74ACT11620 . . . DW OR NT PACKAGE



54ACT11620 . . . FK PACKAGE



NC—No internal connection

FUNCTION TABLE

ENABLE INPUTS		OPERATION
GBA	GAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus

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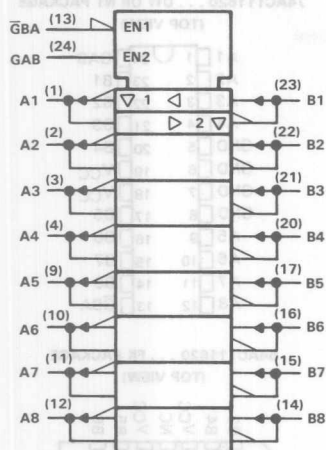
2

Advanced CMOS Circuits

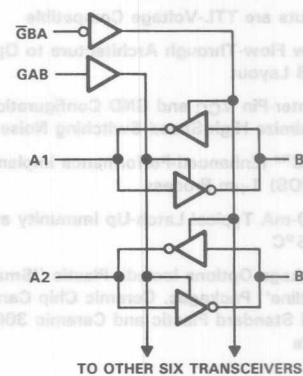
PRODUCT PREVIEW

54ACT11620, 74ACT11620 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±200 mA
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

A and B at state A	H	H
not both	L	H
just A or state B	H	L
just B or at state A	L	L

2

Advanced CMOS Circuits

PRODUCT PREVIEW

54ACT11620, 74ACT11620
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	TEST CONDITIONS	V _{CC}	54ACT11620			74ACT11620			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V
		V _{CC} = 5.5 V	3.85			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V			1.35			1.35	V
		V _{CC} = 5.5 V			1.65			1.65	
I _{OH}	High-level output current	V _{CC} = 4.5 V			-24			-24	mA
		V _{CC} = 5.5 V			-24			-24	
I _{OL}	Low-level output current	V _{CC} = 4.5 V			24			24	mA
		V _{CC} = 5.5 V			24			24	
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise or fall rate		0		10	0		10	ns/V
T _A	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11620		74ACT11620		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1	0.1		0.1		V
		5.5 V			0.1	0.1		0.1		
	I _{OL} = 24 mA	4.5 V			0.36	0.5		0.44		
		5.5 V			0.36	0.5		0.44		
	I _{OL} = 50 mA [†]	5.5 V				1.65				
I _{OZ}	I _{OL} = 75 mA [†]	5.5 V						1.65		μA
	V _O = V _{CC} or GND	5.5 V			±0.5	±10		±5		
I _I	V _I = V _{CC} or GND	5.5 V			±0.1	±1		±1		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4	80		40		μA
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.9	1		1		mA
C _i	V _I = V _{CC} or GND	5 V		4						pF
C _O	V _O = V _{CC} or GND	5 V		10						pF

[†]Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡]This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

2

PRODUCT PREVIEW Advanced CMOS Circuits

54ACT11620, 74ACT11620 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11620		74ACT11620		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A		5.5						ns
t_{PHL}				5.7						
t_{PZH}	$\overline{\text{G}}\text{BA}$	A		6.1						ns
t_{PZL}				7.1						
t_{PHZ}	$\overline{\text{G}}\text{BA}$	A		7.8						ns
t_{PLZ}				7.6						
t_{PZH}	GAB	B		6.4						ns
t_{PZL}				7.8						
t_{PHZ}	GAB	B		7.2						ns
t_{PLZ}				7.1						

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	45	pF
		Outputs disabled		12	

2

Advanced CMOS Circuits

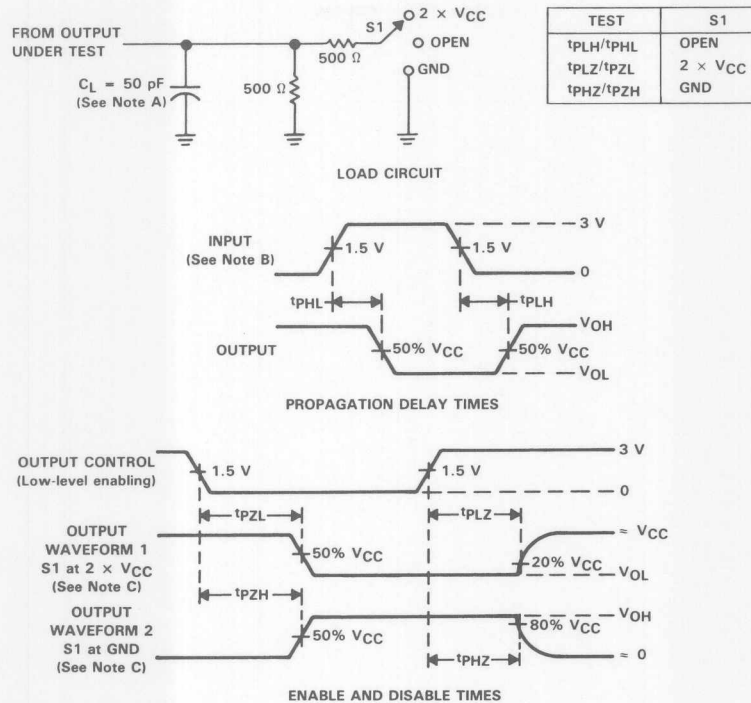
WEIWA9P TCUOD9P

UNIT	54ACT11620	74ACT11620	$T_A = 25^\circ\text{C}$			V _{CC}	TEST CONDITIONS	PARAMETER
V	MAX	MAX	MIN	TYP	MAX	4.5 V	$I_{OH} = -80\text{ }\mu\text{A}$	I_{OH}
	4.5	4.5	4.5	4.5	4.5	4.5 V	$I_{OH} = -80\text{ }\mu\text{A}$	
	4.2	4.2	4.2	4.2	4.2	4.5 V	$I_{OH} = -80\text{ }\mu\text{A}$	
	3.8	3.8	3.8	3.8	3.8	4.5 V	$I_{OH} = -80\text{ }\mu\text{A}$	
	4.3	4.3	4.3	4.3	4.3	4.5 V	$I_{OH} = -80\text{ }\mu\text{A}$	
	3.8	3.8	3.8	3.8	3.8	4.5 V	$I_{OH} = -80\text{ }\mu\text{A}$	
V	1.0	1.0	1.0	1.0	1.0	4.5 V	$I_{OL} = 80\text{ }\mu\text{A}$	I_{OL}
	1.0	1.0	1.0	1.0	1.0	4.5 V	$I_{OL} = 80\text{ }\mu\text{A}$	
	0.5	0.5	0.5	0.5	0.5	4.5 V	$I_{OL} = 80\text{ }\mu\text{A}$	
	0.5	0.5	0.5	0.5	0.5	4.5 V	$I_{OL} = 80\text{ }\mu\text{A}$	
	1.0	1.0	1.0	1.0	1.0	4.5 V	$I_{OL} = 80\text{ }\mu\text{A}$	
	1.0	1.0	1.0	1.0	1.0	4.5 V	$I_{OL} = 80\text{ }\mu\text{A}$	
A_{OL}	0.5	0.5	0.5	0.5	0.5	4.5 V	$V_O = V_{CC}$ or GND	A_{OL}
F_{OL}	1	1	1	1	1	4.5 V	$V_I = V_{CC}$ or GND	F_{OL}
A_{OL}	0.5	0.5	0.5	0.5	0.5	4.5 V	$V_I = V_{CC}$ or GND	A_{OL}
A_{OL}	1	1	1	1	1	4.5 V	$V_I = V_{CC}$ or GND	A_{OL}
t_{PL}						4.5 V	$V_I = V_{CC}$ or GND	t_{PL}
t_{PH}						4.5 V	$V_I = V_{CC}$ or GND	t_{PH}

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

54ACT11620, 74ACT11620
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION

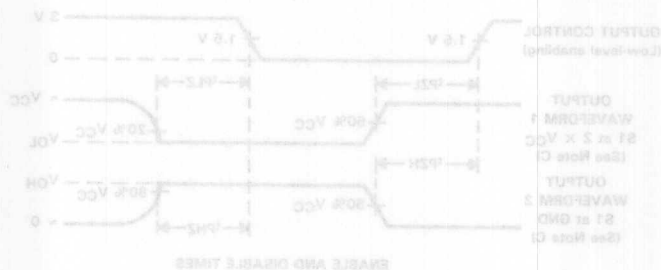


- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

Waveform 1 is for an output with internal conditions such that the output is high except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 3 is for an output with internal conditions such that the output is high except when disabled by the output control. Waveform 4 is for an output with internal conditions such that the output is low except when disabled by the output control.



PROPAGATION DELAY TIMES



LOAD CIRCUIT



PARAMETER MEASUREMENT INFORMATION

TEST	TEST
WAVEFORM 1	WAVEFORM 2
WAVEFORM 3	WAVEFORM 4
WAVEFORM 5	WAVEFORM 6

54AC11623, 74AC11623 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2957, JULY 1987

- Local Bus-Latch Capability
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus, or from the B bus to the A bus, depending upon the logic levels at the enable inputs (GBA and GAB).

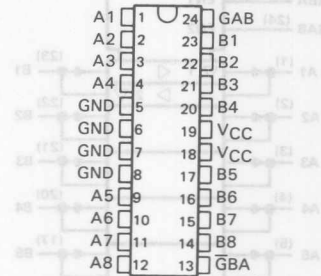
The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of \overline{GBA} and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the AC11623.

The 54AC11623 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC11623 is characterized for operation from -40°C to 85°C.

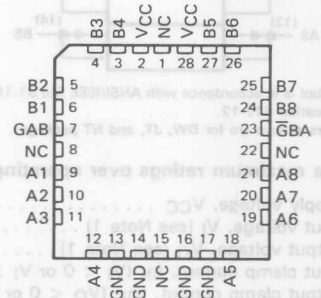
54AC11623 . . . JT PACKAGE
74AC11623 . . . DW OR NT PACKAGE

(TOP VIEW)



54AC11623 . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

ENABLE INPUTS		OPERATION
\overline{GBA}	GAB	
L	L	\overline{B} data to A bus
H	H	\overline{A} data to B bus
H	L	Isolation
L	H	\overline{B} data to A bus, \overline{A} data to B bus

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TEXAS
INSTRUMENTS

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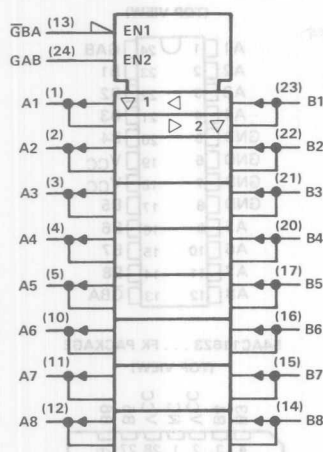
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Advanced CMOS Circuits

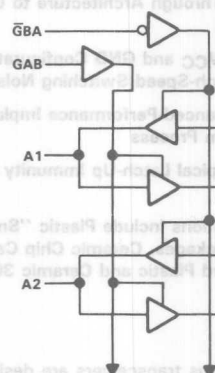
PRODUCT PREVIEW

54AC11623, 74AC11623 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

and B data or B data	H	H
and A data or A data	L	H
and B data or B data	H	L
and A data or A data	H	L

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Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11623, 74AC11623 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

			54AC11623			74AC11623			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1			2.1			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 5.5 V	3.85			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V			0.9			0.9	V
		V _{CC} = 4.5 V			1.35			1.35	
		V _{CC} = 5.5 V			1.65			1.65	
I _{OH}	High-level output current	V _{CC} = 3 V			-4			-4	mA
		V _{CC} = 4.5 V			-24			-24	
		V _{CC} = 5.5 V			-24			-24	
I _{OL}	Low-level output current	V _{CC} = 3 V			12			12	mA
		V _{CC} = 4.5 V			24			24	
		V _{CC} = 5.5 V			24			24	
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise or fall rate		0		10	0		10	ns/V
T _A	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11623		74AC11623		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA [†]	5.5 V				1.65				
I _{OZ}	V _O = V _{CC} or GND	3 V			0.1		0.1		0.1	μA
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _I = V _{CC} or GND	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 75 mA [†]	5.5 V				1.65			1.65	
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±10		±5	μA
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μA
C _i	V _I = V _{CC} or GND	5 V		4						pF
C _o	V _O = V _{CC} or GND	5 V		10						pF

[†]Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

54AC11623, 74AC11623
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C			54AC11623		74AC11623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	3.3 ± 0.3 V		4.1						ns
t _{PHL}			5 ± 0.5 V								
			3.3 ± 0.3 V		4.5						
			5 ± 0.5 V								
t _{PZH}	\overline{G} BA	A	3.3 ± 0.3 V		4.5						ns
t _{PZL}			5 ± 0.5 V		5.1						
			3.3 ± 0.3 V		5.6						
			5 ± 0.5 V		5.7						
t _{PHZ}	\overline{G} BA	A	3.3 ± 0.3 V		5.6						ns
t _{PLZ}			5 ± 0.5 V		5.7						
			3.3 ± 0.3 V		4.9						
			5 ± 0.5 V		5.6						
t _{PZH}	GAB	B	3.3 ± 0.3 V		5.5						ns
t _{PZL}			5 ± 0.5 V		5.6						
			3.3 ± 0.3 V		5.5						
			5 ± 0.5 V		5.6						

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER				TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per transceiver			Outputs enabled	C _L = 50 pF, f = 1 MHz	45	pF
				Outputs disabled		12	
V	0.2	0.2	0.2	0.2	V 0.2		HOV
	0.5	0.5	0.5	0.5	V 0.5		
	0.5	0.5	0.5	0.5	V 0.5		
	0.5	0.5	0.5	0.5	V 0.5		
	0.5	0.5	0.5	0.5	V 0.5		
V	1.0	1.0	1.0	1.0	V 1.0		JOV
	1.0	1.0	1.0	1.0	V 1.0		
	1.0	1.0	1.0	1.0	V 1.0		
	1.0	1.0	1.0	1.0	V 1.0		
	1.0	1.0	1.0	1.0	V 1.0		
	1.0	1.0	1.0	1.0	V 1.0		
	1.0	1.0	1.0	1.0	V 1.0		
	1.0	1.0	1.0	1.0	V 1.0		
	1.0	1.0	1.0	1.0	V 1.0		
	1.0	1.0	1.0	1.0	V 1.0		
V	0.2	0.2	0.2	0.2	V 0.2		JOV
	0.5	0.5	0.5	0.5	V 0.5		
	0.5	0.5	0.5	0.5	V 0.5		
	0.5	0.5	0.5	0.5	V 0.5		
	0.5	0.5	0.5	0.5	V 0.5		
A ₀	0.2	0.2	0.2	0.2	V 0.2		JOV
A ₁	1.0	1.0	1.0	1.0	V 1.0		JOV
A ₂	0.5	0.5	0.5	0.5	V 0.5		JOV
A ₃	0.5	0.5	0.5	0.5	V 0.5		JOV
A ₄	0.5	0.5	0.5	0.5	V 0.5		JOV

not more than one output should be loaded at a time, and the duration of the test should not exceed 10 ms.

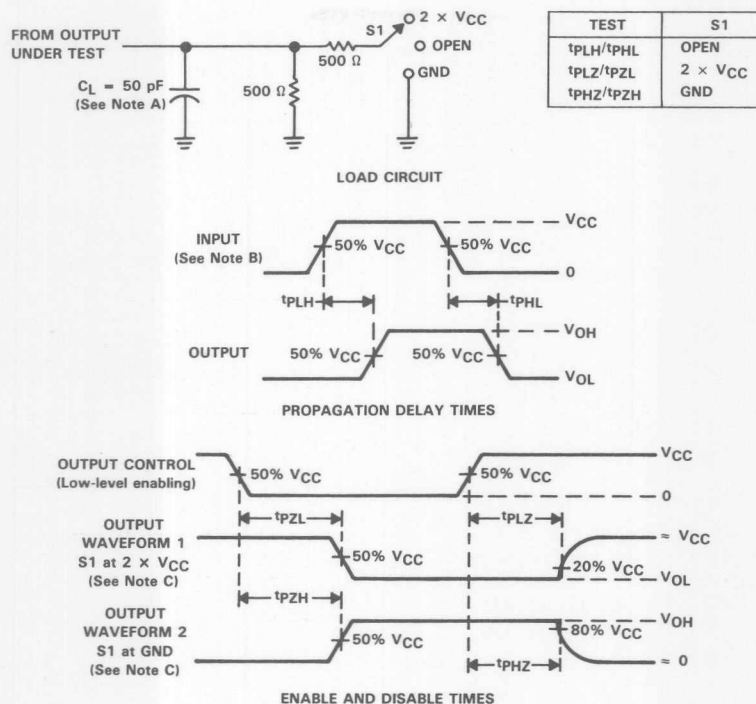
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Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11623, 74AC11623 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

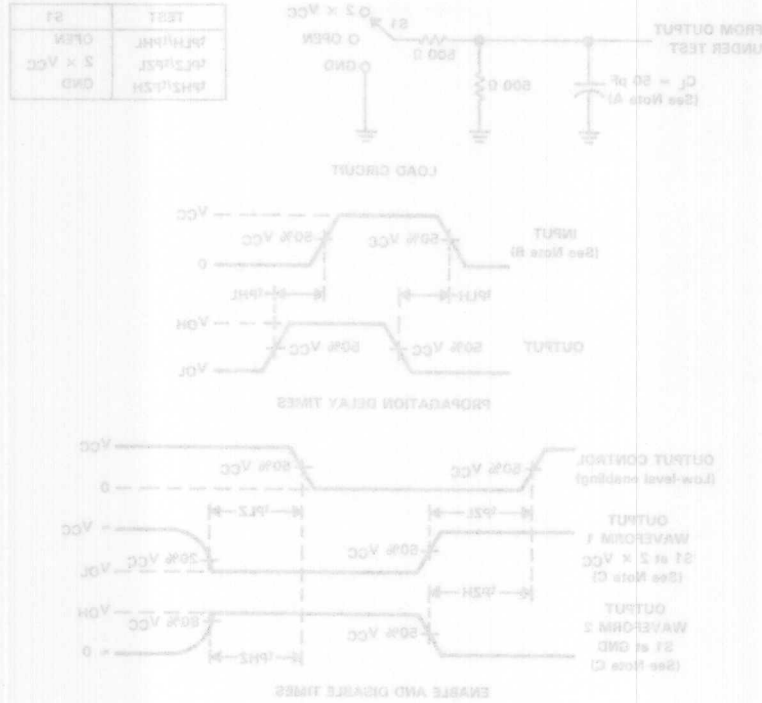
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $r_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. Waveform 3 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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WAVEFORM TUDODRQ

54ACT11623, 74ACT11623 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2957, JULY 1987

- Local Bus-Latch Capability
- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

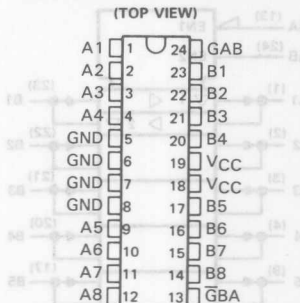
These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}BA$ and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

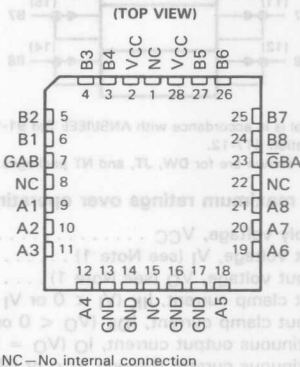
The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of $\overline{G}BA$ and GAB . Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the ACT11623.

The 54ACT11623 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11623 is characterized for operation from -40°C to 85°C.

54ACT11623 . . . JT PACKAGE
74ACT11623 . . . DW OR NT PACKAGE



54ACT11623 . . . FK PACKAGE



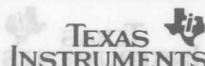
NC—No internal connection

FUNCTION TABLE

ENABLE INPUTS		OPERATION
$\overline{G}BA$	GAB	
L	L	\overline{B} data to A bus
H	H	\overline{A} data to B bus
H	L	Isolation
L	H	\overline{B} data to A bus, \overline{A} data to B bus

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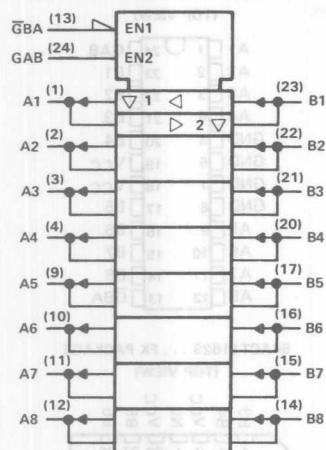
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Advanced CMOS Circuits

PRODUCT PREVIEW

54ACT11623, 74ACT11623 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

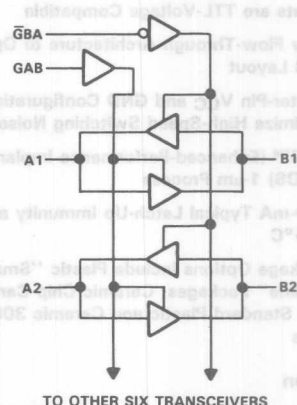
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



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Advanced CMOS Circuits

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

A data to B bus	H	H
Isolation	L	H
B data to A bus	H	L
A data to B bus	H	L

54ACT11623, 74ACT11623
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	TEST CONDITIONS	V _{CC}	54ACT11623			74ACT11623			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V V _{CC} = 5.5 V	3.15 3.85			3.15 3.85			V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V V _{CC} = 5.5 V			1.35 1.65			1.35 1.65	V
I _{OH}	High-level output current	V _{CC} = 4.5 V V _{CC} = 5.5 V			-24 -24			-24 -24	mA
I _{OL}	Low-level output current	V _{CC} = 4.5 V V _{CC} = 5.5 V			24 24			24 24	mA
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise or fall rate		0		10	0		10	ns/V
T _A	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11623		74ACT11623		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†] I _{OH} = -75 mA [†]	5.5 V 5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1	0.1		0.1		V
		5.5 V			0.1	0.1		0.1		
	I _{OL} = 24 mA	4.5 V			0.36	0.5		0.44		
		5.5 V			0.36	0.5		0.44		
	I _{OL} = 50 mA [†] I _{OL} = 75 mA [†]	5.5 V 5.5 V				1.65				
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5	±10		±5		μA
I _I	V _I = V _{CC} or GND	5.5 V			±0.1	±1		±1		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4	80		40		μA
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.9	1		1		mA
C _i	V _I = V _{CC} or GND	5 V			4					pF
C _O	V _O = V _{CC} or GND	5 V			10					pF

[†]Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡]This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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PRODUCT PREVIEW

54ACT11623, 74ACT11623
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11623		74ACT11623		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A		5.2						ns
t_{PHL}				5.7						
t_{PZH}	\bar{G} BA	A		6						ns
t_{PZL}				7						
t_{PHZ}	\bar{G} BA	A		7.8						ns
t_{PLZ}				7.6						
t_{PZH}	GAB	B		6.4						ns
t_{PZL}				7.4						
t_{PHZ}	GAB	B		7.2						ns
t_{PLZ}				7						

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	45	pF
		Outputs disabled		12	

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Advanced CMOS Circuits

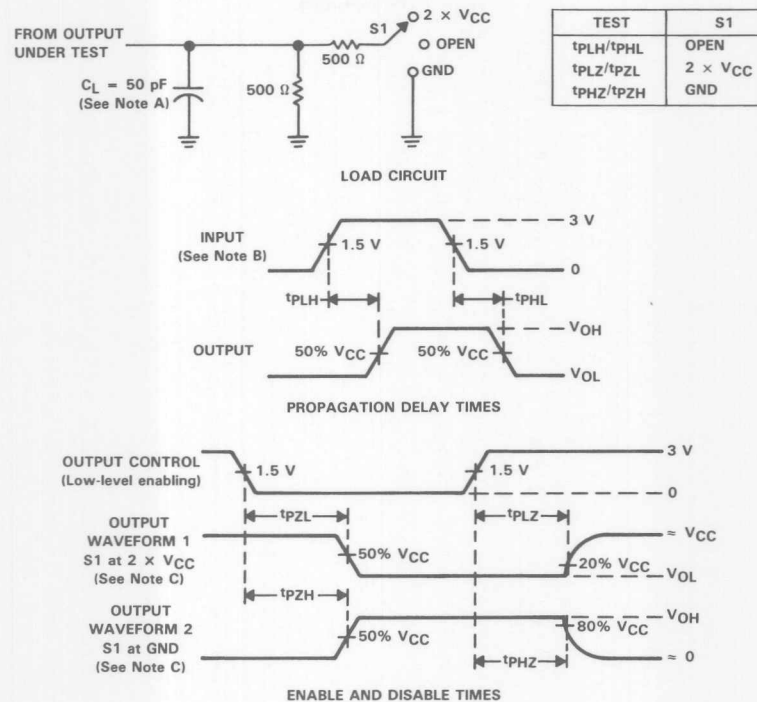
PRODUCT PREVIEW

UNIT	PARAMETER		TEST CONDITIONS		$T_A = 25^\circ\text{C}$		V_{CC}	TEST CONDITIONS	PARAMETER
	MIN	MAX	MIN	MAX	MIN	TYP			
V	4.5	4.5	4.5	4.5	4.5	4.5	4.5 V	$I_{OH} = -50\text{ }\mu\text{A}$	V_{OH}
V	0.45	0.45	0.45	0.45	0.45	0.45	4.5 V	$I_{OL} = 50\text{ }\mu\text{A}$	V_{OL}
A ₁	0.5	0.5	0.5	0.5	0.5	0.5	4.5 V	$V_I = V_{CC}$ or GND	I_{CC}
A ₂	0.5	0.5	0.5	0.5	0.5	0.5	4.5 V	$V_I = V_{CC}$ or GND	I_{CC}
A ₃	0.5	0.5	0.5	0.5	0.5	0.5	4.5 V	$V_I = V_{CC}$ or GND	I_{CC}
A ₄	0.5	0.5	0.5	0.5	0.5	0.5	4.5 V	$V_I = V_{CC}$ or GND	I_{CC}
A ₅	0.5	0.5	0.5	0.5	0.5	0.5	4.5 V	$V_I = V_{CC}$ or GND	I_{CC}
A ₆	0.5	0.5	0.5	0.5	0.5	0.5	4.5 V	$V_I = V_{CC}$ or GND	I_{CC}
A ₇	0.5	0.5	0.5	0.5	0.5	0.5	4.5 V	$V_I = V_{CC}$ or GND	I_{CC}

Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms. This is the increase in supply current for each input that is one of the specified TTL voltage levels rather than 0 V or V_{CC} .

54ACT11623, 74ACT11623 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. Input pulses are supplied by generators having the following characteristics: PRR \leq MHz, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = \text{ns}$.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54AC11640, 74AC11640 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2957, JULY 1987

- Bidirectional Bus Transceivers in High-Density 24-Pin Packages
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

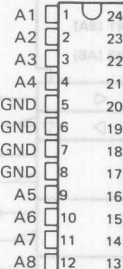
description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input \bar{G} can be used to disable the device so the buses are effectively isolated.

The 54AC11640 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74AC11640 is characterized for operation from -40°C to 85°C .

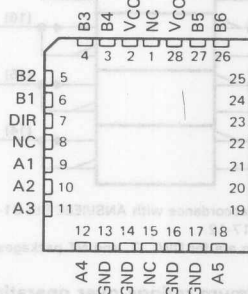
54AC11640 ... JT PACKAGE
74AC11640 ... DW OR NT PACKAGE

(TOP VIEW)



54AC11640 ... FK PACKAGE

(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

CONTROL INPUTS		OPERATION
\bar{G}	DIR	
L	L	\bar{B} data to A bus
L	H	\bar{A} data to B bus
H	X	Isolation

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TEXAS
INSTRUMENTS

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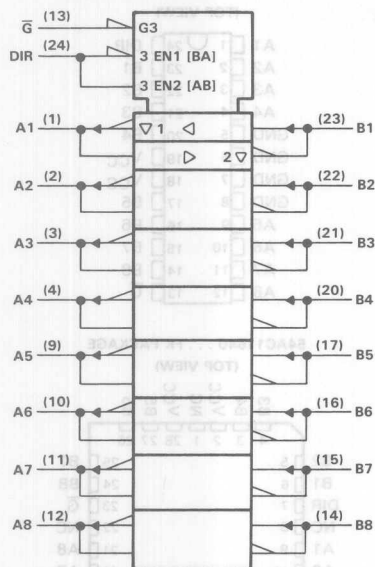
2

Advanced CMOS Circuits

PRODUCT PREVIEW

WITH 3-STATE OUTPUTS

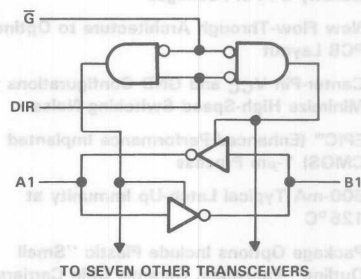
logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

2

Advanced CMOS Circuits

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input diode current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output diode current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

²Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54AC11640, 74AC11640
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

recommended operating conditions

		54AC11640			74AC11640			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V _{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1			2.1			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 5.5 V	3.85			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V			0.9			0.9	V
		V _{CC} = 4.5 V			1.35			1.35	
		V _{CC} = 5.5 V			1.65			1.65	
I _{OH}	High-level output current	V _{CC} = 3 V			-4			-4	mA
		V _{CC} = 4.5 V			-24			-24	
		V _{CC} = 5.5 V			-24			-24	
I _{OL}	Low-level output current	V _{CC} = 3 V			12			12	mA
		V _{CC} = 4.5 V			24			24	
		V _{CC} = 5.5 V			24			24	
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise or fall rate	\overline{G} or DIR	0		5	0		5	ns/V
		Data	0		10	0		10	
T _A	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics (see Figure 1)

UNIT			V _{CC}	TO	FROM	PARAMETER
ns			3.0 ± 0.3 V	A to B	A to B	t _{PLH}
			5.0 ± 0.3 V			
ns			3.0 ± 0.3 V	A to B	A to B	t _{PHL}
			5.0 ± 0.3 V			
ns			3.0 ± 0.3 V	A to B	\overline{B}	t _{PLH}
			5.0 ± 0.3 V			
ns			3.0 ± 0.3 V	A to B	\overline{B}	t _{PHL}
			5.0 ± 0.3 V			
ns			3.0 ± 0.3 V	A to B	\overline{B}	t _{PLH}
			5.0 ± 0.3 V			
ns			3.0 ± 0.3 V	A to B	\overline{B}	t _{PHL}
			5.0 ± 0.3 V			

operating characteristics, V_{CC} = 5 V, T_A = 25°C

UNIT	TYP	TEST CONDITIONS	PARAMETER
dB	45	C _L = 50 pF, f = 1 MHz	Output enabled
	15		Output disabled

54AC11640, 74AC11640 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11640		74AC11640		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
	I _{OH} = -24 mA	5.5 V	4.94			4.7		4.8		
		5.5 V				3.85				
V _{OL}	I _{OL} = 50 µA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
	I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	
		5.5 V								
I _{OZ}	V _O = V _{CC} or GND	3 V								µA
		4.5 V								
		5.5 V								
	I _{OZ} = 50 mA†	5.5 V				1.65				
		5.5 V						1.65		
	I _{OZ} = 75 mA†	5.5 V								
		5.5 V								
I _I	V _I = V _{CC} or GND	5.5 V			±0.5		±10		±5	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	µA
C _i	V _I = V _{CC} or GND	5 V			4					pF
C _o	V _O = V _{CC} or GND	5 V			10					pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C			54AC11640		74AC11640		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.9						
t _{PHL}	A or B	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.8						
t _{PZH}	\bar{G}	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		7.7						
t _{PZL}	\bar{G}	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		7.4						
t _{PHZ}	\bar{G}	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		8.4						
t _{PLZ}	\bar{G}	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		8						

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C _L = 50 pF, f = 1 MHz	45	pF
		Outputs disabled		12	

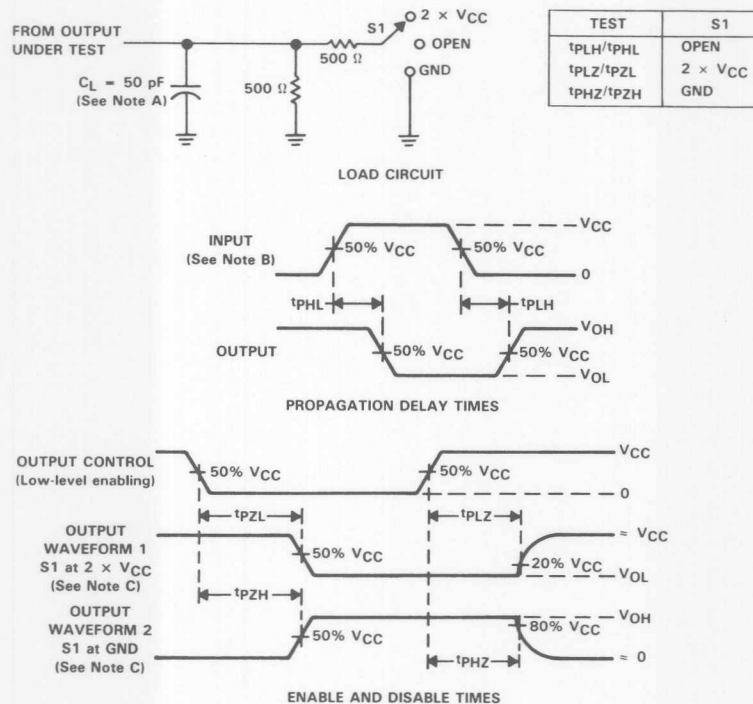
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Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11640, 74AC11640 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION

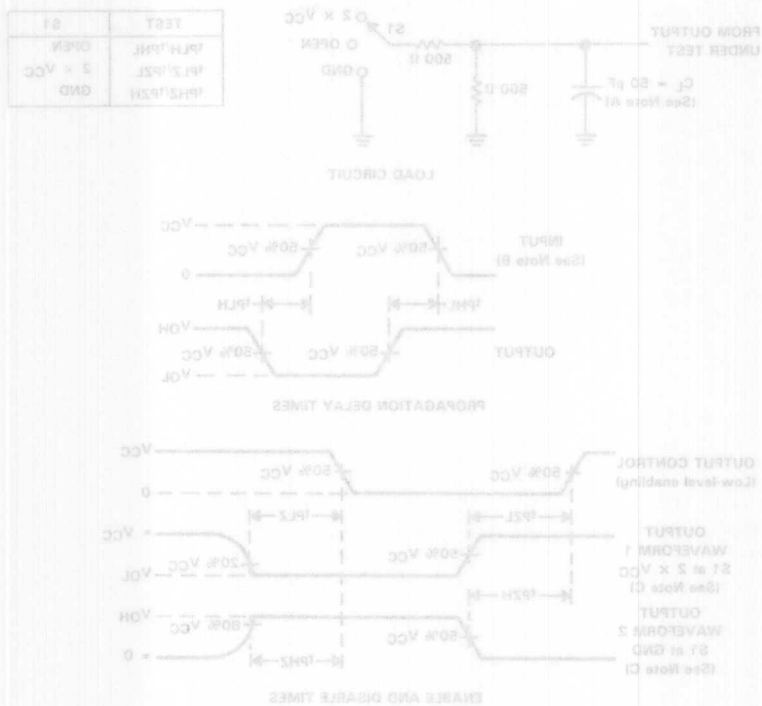


FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

NOTES:
A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $t_r = 20 \text{ pF}$, $t_f = 3 \text{ ns}$, $t_d = 3 \text{ ns}$.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

54ACT11640, 74ACT11640 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2957, JULY 1987—REVISED SEPTEMBER 1987

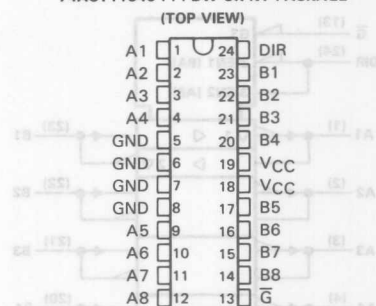
- Bidirectional Bus Transceivers in High-Density 24-Pin Packages
- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

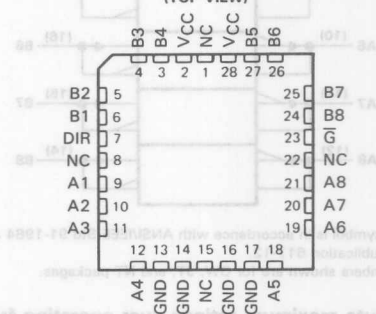
These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input \bar{G} can be used to disable the device so the buses are effectively isolated.

The 54ACT11640 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11640 is characterized for operation from -40°C to 85°C.

54ACT11640 ... JT PACKAGE
74ACT11640 ... DW OR NT PACKAGE



54ACT11640 ... FK PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

CONTROL INPUTS		OPERATION
\bar{G}	DIR	
L	L	\bar{B} data to A bus
L	H	\bar{A} data to B bus
H	X	Isolation

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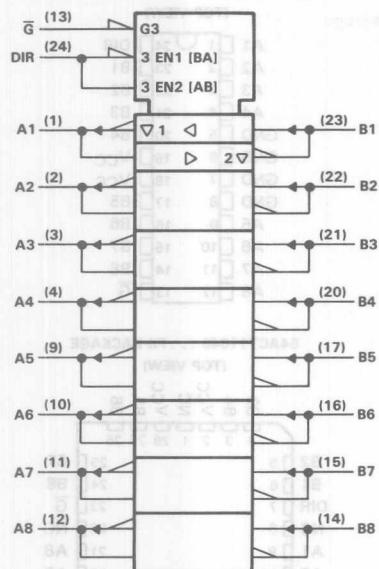
TEXAS
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54ACT11640, 74ACT11640 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

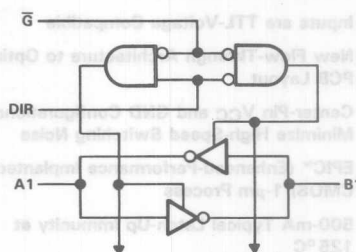
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



TO SEVEN OTHER TRANSCEIVERS

Pin numbers shown are for DW, JT, and NT packages.

2

Advanced CMOS Circuits

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input diode current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output diode current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54ACT11640, 74ACT11640 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

		54ACT11640			74ACT11640			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-24			-24	mA
I _{OL}	Low-level output current			24			24	mA
V _I	Input voltage	0		V _{CC}	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise or fall rate	0		10	0		10	ns/V
T _A	Operating free-air temperature	-55		125	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11640		74ACT11640		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA†	5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	4.5 V		0.1		0.1		0.1		V
		5.5 V		0.1		0.1		0.1		
	I _{OL} = 24 mA	4.5 V		0.36		0.5		0.44		
		5.5 V		0.36		0.5		0.44		
	I _{OL} = 50 mA†	5.5 V				1.65				
I _{OZ}	A or B Ports	V _O = V _{CC} or GND	5.5 V		±0.5	±10		±5		μA
		V _I = V _{CC} or GND	5.5 V		±0.1	±1		±1		
	I _I	V _I = V _{CC} or GND, I _O = 0	5.5 V		8	160		80		
		One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V		0.9	1		1		
	ΔI _{CC} ‡									
C _i	̄ or DIR	V _I = V _{CC} or GND	5 V		4					pF
C _{io}	A or B Ports	V _O = V _{CC} or GND	5 V		12					pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics V_{CC} = 5 V ± 0.5 V, (see Figure 1)

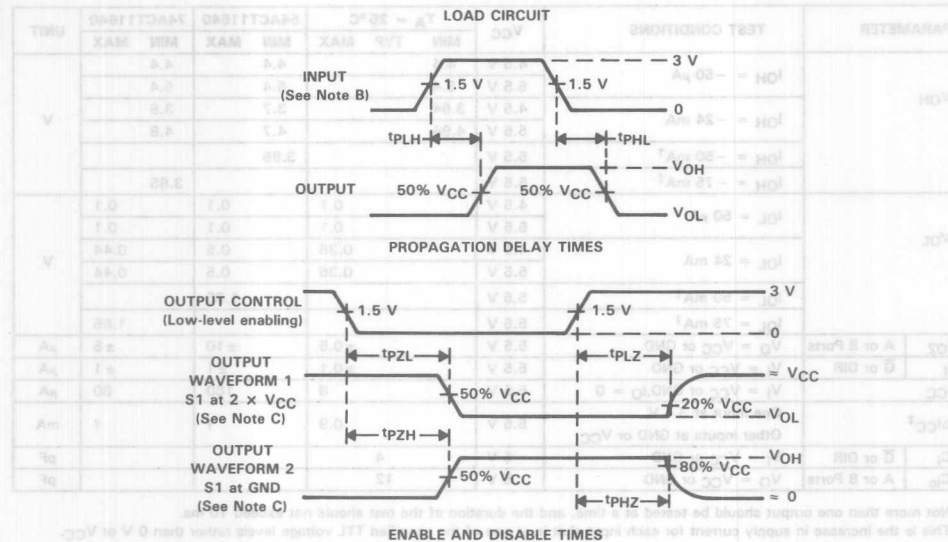
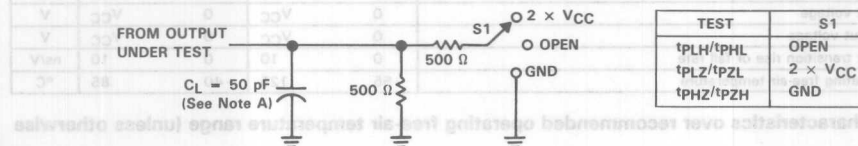
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54ACT11640		74ACT11640		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	1.5	6.3	9.6	1.5	11	1.5	10.5	ns
t _{PHL}			1.5	5.7	8.6	1.5	10	1.5	9.5	
t _{PZH}	̄	A or B	1.5	8.8	12.2	1.5	14.2	1.5	13.4	ns
t _{PZL}			1.5	8.4	12.3	1.5	14.5	1.5	13.6	
t _{PHZ}	̄	A or B	1.5	9.1	12.9	1.5	14.5	1.5	13.9	ns
t _{PLZ}			1.5	9.6	13.1	1.5	15	1.5	14.2	

54ACT11640, 74ACT11640 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per transceiver	Outputs enabled	45	pF
	Outputs disabled	12	

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_0 = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

54AC11643, 74AC11643 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2957, JULY 1987

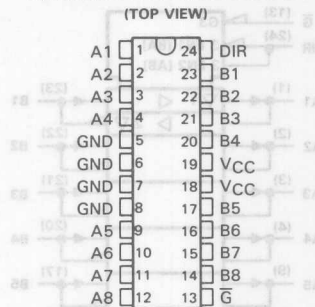
- Bidirectional Bus Transceivers in High-Density 24-Pin Packages
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

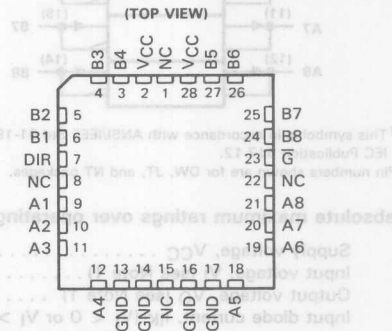
These octal transceivers are designed for asynchronous, two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (\bar{G}) can be used to disable the device so the buses are effectively isolated.

The 54AC11643 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC11643 is characterized for operation from -40°C to 85°C.

54AC11643 . . . JT PACKAGE
74AC11643 . . . DW OR NT PACKAGE



54AC11643 . . . FK PACKAGE



NC—No internal connection

FUNCTION TABLE

CONTROL INPUTS		OPERATION
\bar{G}	DIR	
L	L	B data to A bus
L	H	\bar{A} data to B bus
H	X	Isolation

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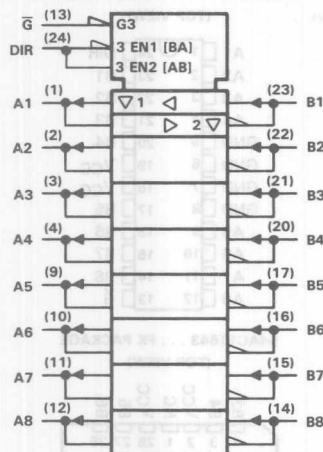


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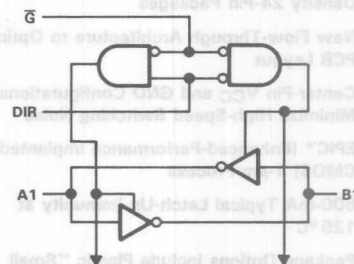
54AC11643, 74AC11643 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



TO SEVEN OTHER TRANSCEIVERS

Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input diode current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output diode current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

and B to state A	L	H
isolation	H	X

2

Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11643, 74AC11643
OCTAL BUSS TRANSCEIVERS
WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	TEST CONDITIONS	V _{CC}	54AC11643			74AC11643			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1			2.1			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 5.5 V	3.85			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V			0.9			0.9	V
		V _{CC} = 4.5 V			1.35			1.35	
		V _{CC} = 5.5 V			1.65			1.65	
I _{OH}	High-level output current	V _{CC} = 3 V			-4			-4	mA
		V _{CC} = 4.5 V			-24			-24	
		V _{CC} = 5.5 V			-24			-24	
I _{OL}	Low-level output current	V _{CC} = 3 V			12			12	mA
		V _{CC} = 4.5 V			24			24	
		V _{CC} = 5.5 V			24			24	
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise or fall rate	⎯ or DIR	0		5	0		5	ns/V
		Data	0		10	0		10	
T _A	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11643		74AC11643		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
	I _{OH} = -75 mA [†]	5.5 V						3.85		
V _{OL}	I _{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA [†]	5.5 V				1.65				
	I _{OL} = 75 mA [†]	5.5 V						1.65		
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±10		±5	μA
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μA
C _i	V _I = V _{CC} or GND	5 V			4					pF
C _O	V _O = V _{CC} or GND	5 V			10					pF

[†]Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

2

Advanced CMOS Circuits

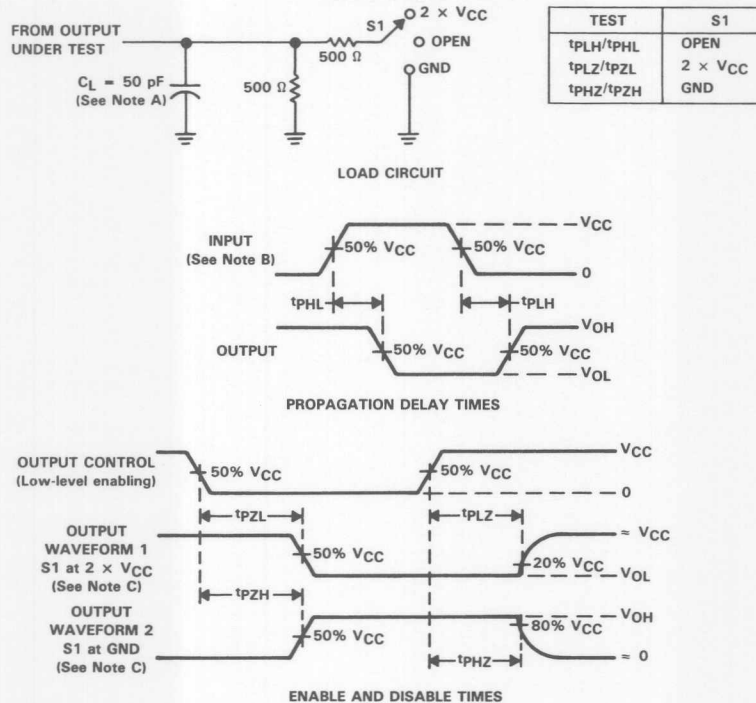
PRODUCT PREVIEW

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25 °C			54AC11643		74AC11643		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	3.3 ± 0.3 V 5 ± 0.5 V		4.3						ns
t _{PHL}	A or B	A or B	3.3 ± 0.3 V 5 ± 0.5 V		4.8						ns
t _{PZH}	\overline{G}	A or B	3.3 ± 0.3 V 5 ± 0.5 V		4.7						ns
t _{PZL}	\overline{G}	A or B	3.3 ± 0.3 V 5 ± 0.5 V		5.4						ns
t _{PHZ}	\overline{G}	A or B	3.3 ± 0.3 V 5 ± 0.5 V		6.6						ns
t _{PLZ}	\overline{G}	A or B	3.3 ± 0.3 V 5 ± 0.5 V		6.5						ns

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per transceiver	Outputs enabled	45	pF
		Outputs disabled	12	

54AC11643, 74AC11643
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_0 = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

2

Advanced CMOS Circuits

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

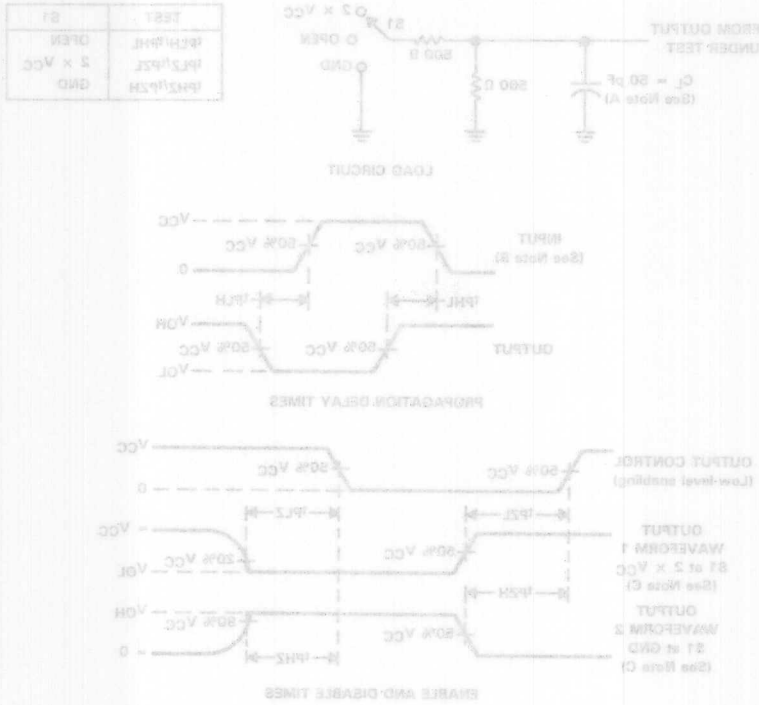


FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $t_r = 50 \text{ pF}$, $t_f = 3 \text{ ns}$, $t_d = 3 \text{ ns}$.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

54ACT11643, 74ACT11643 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2957, JULY 1987

- Bidirectional Bus Transceivers in High-Density 24-Pin Packages
- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

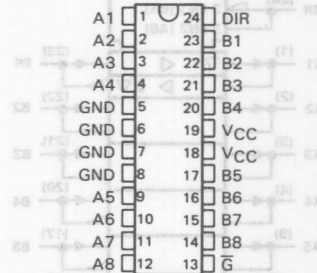
description

These octal bus transceivers are designed for asynchronous, two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input \bar{G} can be used to disable the device so the buses are effectively isolated.

The 54ACT11643 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74ACT11643 is characterized for operation from -40°C to 85°C .

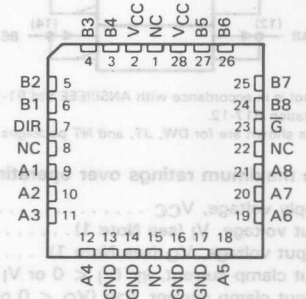
54ACT11643 ... JT PACKAGE
74ACT11643 ... DW OR NT PACKAGE

(TOP VIEW)



54ACT11643 ... FK PACKAGE

(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

CONTROL INPUTS		OPERATION
\bar{G}	DIR	
L	L	\bar{B} data to A bus
L	H	A data to B bus
H	X	Isolation

TYP	54ACT11643			74ACT11643		
	MIN	TYP	MAX	MIN	TYP	MAX
V _{CC}	4.5	5.0	5.5	4.5	5.0	5.5
V _I	0.0	0.8	1.5	0.0	0.8	1.5
V _O	0.0	1.5	5.0	0.0	1.5	5.0
I _{CC}	0	10	20	0	10	20
I _O	0	10	20	0	10	20
t _{PLH}	0	10	20	0	10	20
t _{PHL}	0	10	20	0	10	20
t _{tr}	0	10	20	0	10	20
t _{td}	0	10	20	0	10	20

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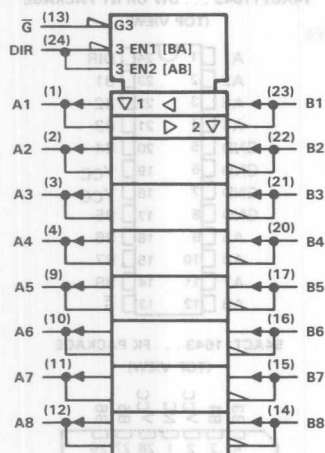
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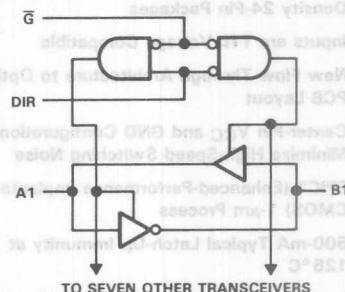
2

Advanced CMOS Circuits

PRODUCT PREVIEW



Pin numbers shown are for DW, JT, and NT packages.



Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

		54ACT11643			74ACT11643			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-24			-24	mA
I _{OL}	Low-level output current			24			24	mA
V _I	Input voltage	0		V _{CC}	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise or fall rate	0		10	0		10	ns/V
T _A	Operating free-air temperature	-55		125	-40		85	°C

54ACT11643, 74ACT11643 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11643		74ACT11643		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1	0.1		0.1		V
		5.5 V			0.1	0.1		0.1		
	I _{OL} = 24 mA	4.5 V			0.36	0.5		0.44		
		5.5 V			0.36	0.5		0.44		
	I _{OL} = 50 mA [†]	5.5 V				1.65				
	I _{OL} = 75 mA [†]	5.5 V						1.65		
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5	±10		±5		μA
I _I	V _I = V _{CC} or GND	5.5 V			±0.1	±1		±1		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8	160		80		μA
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.9	1		1		mA
C _i	V _I = V _{CC} or GND	5 V			4					pF
C _o	V _O = V _{CC} or GND	5 V			10					pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54ACT11643		74ACT11643		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	5.4							ns
t _{PHL}			5.3							
t _{PZH}	A	A or B	5.2							ns
t _{PZL}			6							
t _{PHZ}	A	A or B	6.9							ns
t _{PLZ}			6.8							

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C _L = 50 pF, f = 1 MHz	45	pF
		Outputs disabled		12	

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Advanced CMOS Circuits

PRODUCT PREVIEW

54ACT11643, 74ACT11643 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION

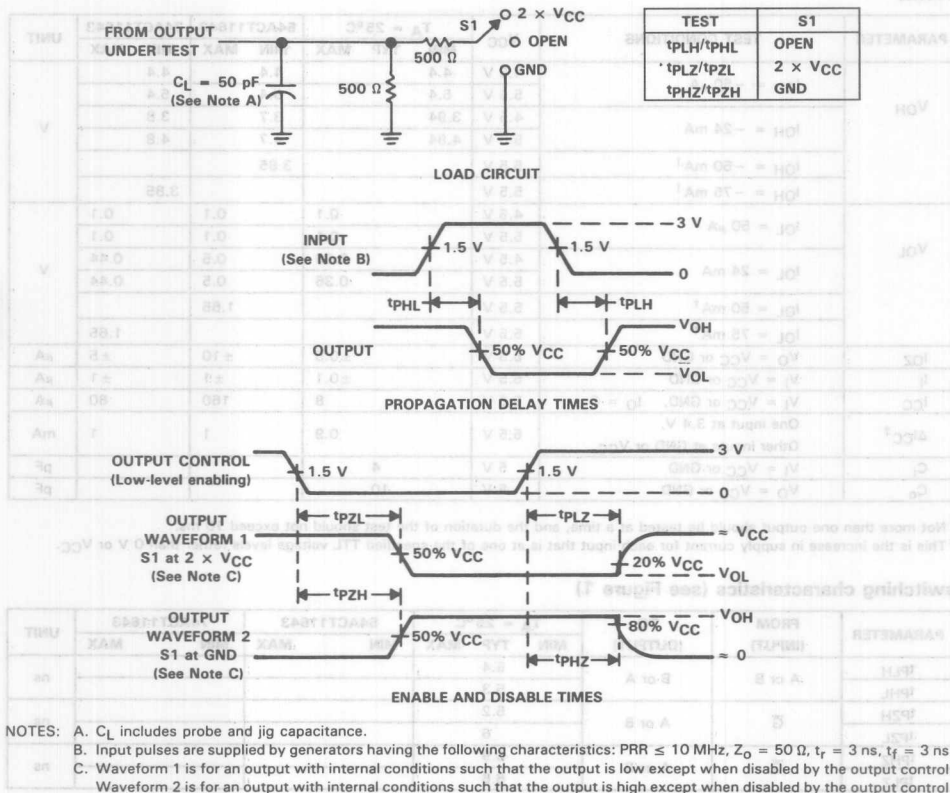


FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

2

Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11646, 74AC11646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

D2957, JULY 1987

- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic DIPs

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry with 3-state outputs arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

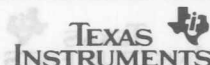
Enable (\bar{G}) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable \bar{G} is active (low). In the isolation mode (control \bar{G} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

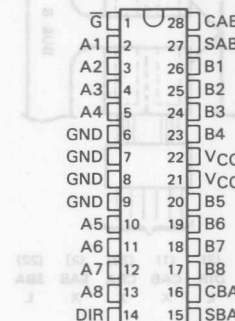
The 54AC11646 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC11646 is characterized for operation from -40°C to 85°C.

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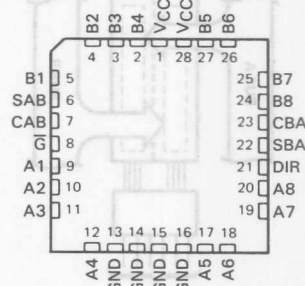
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54AC11646 ... JD PACKAGE
74AC11646 ... DW OR NW PACKAGE
(TOP VIEW)



54AC11646 ... FK PACKAGE
(TOP VIEW)



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
X	X	X	X	1	X	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

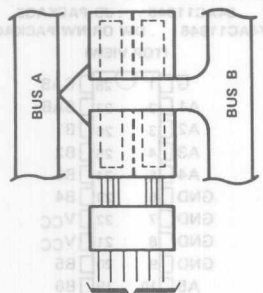
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Advanced CMOS Circuits

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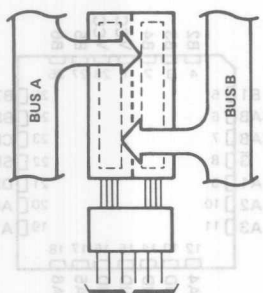
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54AC11646, 74AC11646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS



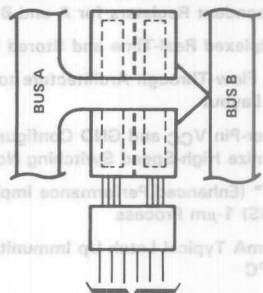
(21)	(3)	(1)	(23)	(2)	(22)
G	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



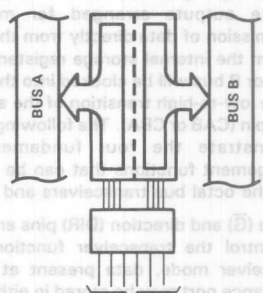
(21)	(3)	(1)	(23)	(2)	(22)
G	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



(21)	(3)	(1)	(23)	(2)	(22)
G	DIR	CAB	CBA	SAB	SBA
L	L	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



(21)	(3)	(1)	(23)	(2)	(22)
G	DIR	CAB	CBA	SAB	SBA
L	L	X	HorL	X	H
L	H	HorL	X	H	X

TRANSFER
STORED DATA
TO A OR B

2

Advanced CMOS Circuits

PRODUCT PREVIEW

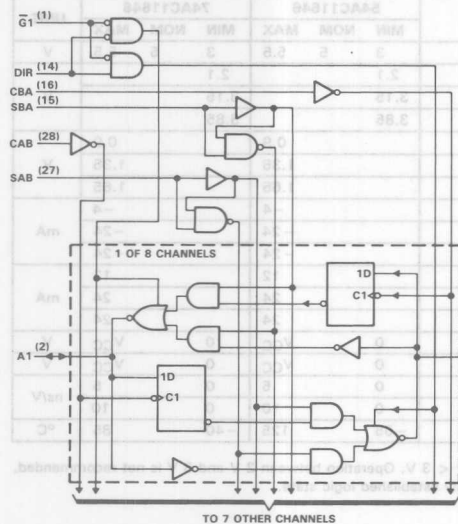
54AC11646, 74AC11646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
G	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored A Data to B Bus

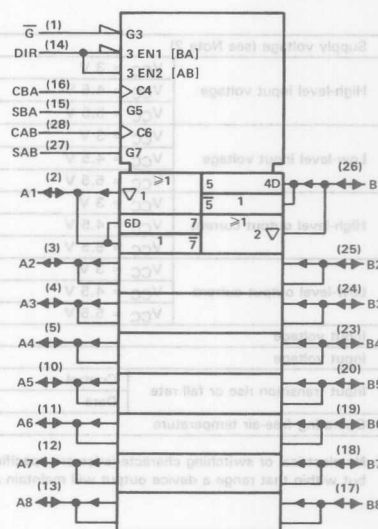
† The data output functions may be enabled or disabled by various signals at the \overline{G} and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

functional block diagram (positive logic)



Pin numbers shown are for DW, JD, and NW packages.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JD, and NW packages.

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Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11646, 74AC11646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to $V_{CC}+0.5$ V
Output voltage, V_O (see Note 1)	−0.5 V to $V_{CC}+0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±200 mA
Storage temperature range	−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11646			74AC11646			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3$ V	2.1			2.1			V
		$V_{CC} = 4.5$ V	3.15			3.15			
		$V_{CC} = 5.5$ V	3.85			3.85			
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V			0.9			0.9	V
		$V_{CC} = 4.5$ V			1.35			1.35	
		$V_{CC} = 5.5$ V			1.65			1.65	
I_{OH}	High-level output current	$V_{CC} = 3$ V			−4			−4	mA
		$V_{CC} = 4.5$ V			−24			−24	
		$V_{CC} = 5.5$ V			−24			−24	
I_{OL}	Low-level output current	$V_{CC} = 3$ V			12			12	mA
		$V_{CC} = 4.5$ V			24			24	
		$V_{CC} = 5.5$ V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Input voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Control	0		5	0		5	ns/V
		Data	0		10	0		10	
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at $V_{CC} < 3$ V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

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Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11646, 74AC11646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11646		74AC11646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
V _{OL}	I _{OH} = -50 mA†	5.5 V				3.85				V
	I _{OH} = -75 mA†	5.5 V						3.85		
I _{OL}	I _{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
I _{OL}	I _{OL} = 24 mA	5.5 V								V
	I _{OL} = 50 mA†	5.5 V				1.65				
I _{OL}	I _{OL} = 75 mA†	5.5 V						1.65		V
	I _{OL} = 75 mA†	5.5 V								
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±10		±5	μA
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μA
C _i	V _I = V _{CC} or GND	5 V		4						pF
C _o	V _O = V _{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements (see Figure 1)

		V _{CC} RANGE	T _A = 25°C		54AC11646		74AC11646		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	3.3 ± 0.3 V							MHz
		5 ± 0.5 V							
t _w	Pulse duration, CAB or CBA high or low	3.3 ± 0.3 V							ns
		5 ± 0.5 V							
t _{su}	Setup time, A before CAB† or B before CBA†	3.3 ± 0.3 V							ns
		5 ± 0.5 V							
t _h	Hold time, A after CAB† or B after CBA†	3.3 ± 0.3 V							ns
		5 ± 0.5 V							

PARAMETER	TEST CONDITIONS	UNIT
C _{in} Power dissipation capacitance per transceiver	C _L = 50 pF, t = 1 MHz	pF
C _{out} Output capacitance		pF

54AC11646, 74AC11646
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC RANGE	TA = 25°C			54AC11646		74AC11646		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			3.3 ± 0.3 V								MHz
			5 ± 0.5 V								
t _{PLH}	A or B	B or A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		4.8						
t _{PHL}			3.3 ± 0.3 V								ns
			5 ± 0.5 V		6						
t _{PZH}	\overline{G}	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		6.1						
t _{PZL}			3.3 ± 0.3 V								ns
			5 ± 0.5 V		8.5						
t _{PHZ}	\overline{G}	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.4						
t _{PLZ}			3.3 ± 0.3 V								ns
			5 ± 0.5 V		5						
t _{PLH}	CBA or CAB	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		7						
t _{PHL}			3.3 ± 0.3 V								ns
			5 ± 0.5 V		8.8						
t _{PLH}	SBA or SAB† (A or B high)	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.6						
t _{PHL}			3.3 ± 0.3 V								ns
			5 ± 0.5 V		6.9						
t _{PLH}	SBA or SAB† (A or B low)	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.6						
t _{PHL}			3.3 ± 0.3 V								ns
			5 ± 0.5 V		6.9						
t _{PZH}	DIR	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		6.4						
t _{PZL}			3.3 ± 0.3 V								ns
			5 ± 0.5 V		8.4						
t _{PHZ}	DIR	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		2.7						
t _{PLZ}			3.3 ± 0.3 V								ns
			5 ± 0.5 V		3.2						

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

operating characteristics, VCC = 5 V, TA = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per transceiver	Outputs enabled	CL = 50 pF, f = 1 MHz	45	pF
		Outputs disabled		12	

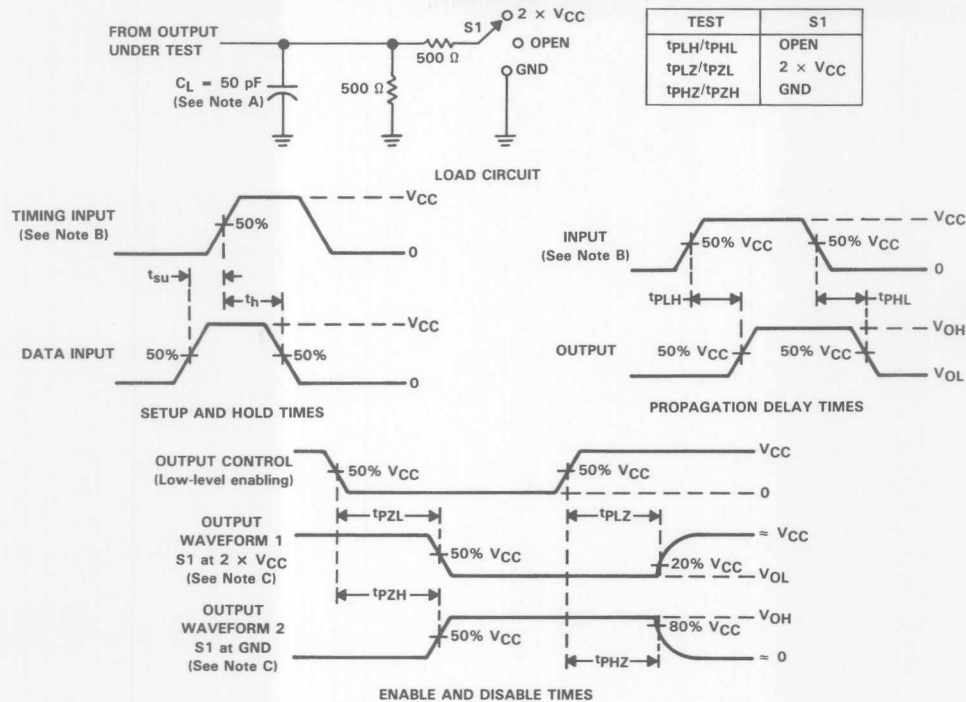
2

Advanced CMOS Circuits

PRODUCT PREVIEW

54AC11646, 74AC11646
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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Advanced CMOS Circuits

PRODUCT PREVIEW

54ACT11646, 74ACT11646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

D2957, JULY 1987

- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic DIPs

description

These devices consist of bus transceiver circuits, 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable (\bar{G}) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable \bar{G} is active (low). In the isolation mode (control \bar{G} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The 54ACT11646 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74ACT11646 is characterized for operation from -40°C to 85°C .

EPIC is a trademark of Texas Instruments Incorporated.

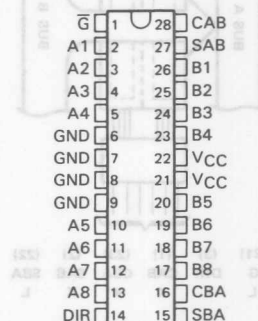
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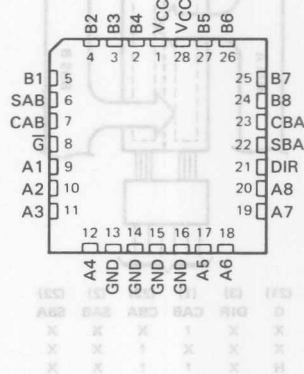
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2-259

54ACT11646 . . . JD PACKAGE
74ACT11646 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11646 . . . FK PACKAGE
(TOP VIEW)



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Advanced CMOS Circuits

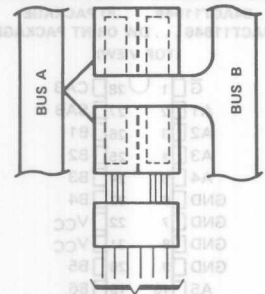
PRODUCT PREVIEW

54ACT11646, 74ACT11646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

2

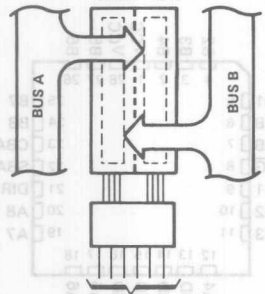
Advanced CMOS Circuits

PRODUCT PREVIEW



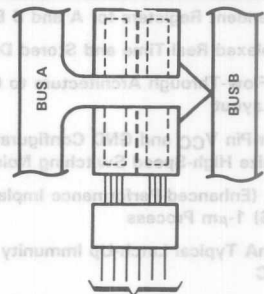
(21)	(3)	(1)	(23)	(2)	(22)
G	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



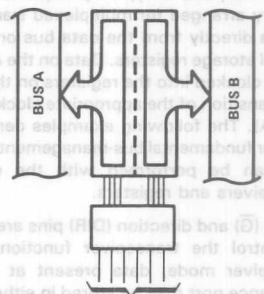
(21)	(3)	(1)	(23)	(2)	(22)
G	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



(21)	(3)	(1)	(23)	(2)	(22)
G	DIR	CAB	CBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



(21)	(3)	(1)	(23)	(2)	(22)
G	DIR	CAB	CBA	SAB	SBA
L	L	X	HorL	X	H
L	H	HorL	X	H	X

TRANSFER
STORED DATA
TO A OR B

The 54ACT11646 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11646 is characterized for operation from -40°C to 85°C.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

54ACT11646, 74ACT11646

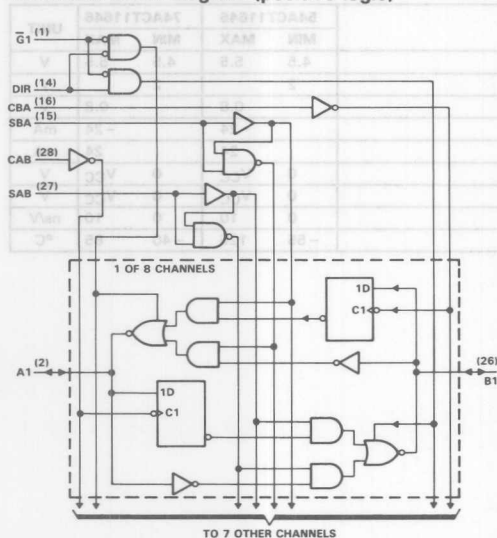
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
G	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified [†]	Store A, B unspecified [†]
X	X	X	↑	X	X	Unspecified [†]	Input	Store B, A unspecified [†]
H	X	↑	↑	X	X			Store A and B Data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

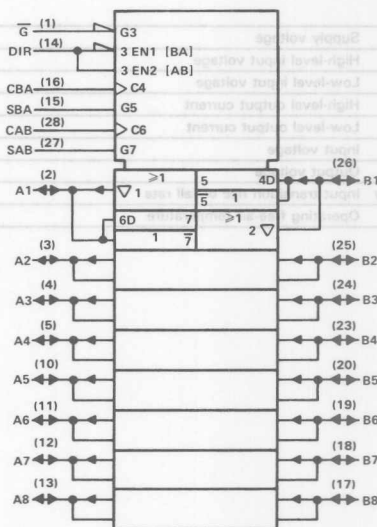
[†] The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

functional block diagram (positive logic)



Pin numbers shown are for DW, JD, and NT packages.

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JD, and NT packages.

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Advanced CMOS Circuits

PRODUCT PREVIEW

54ACT11646, 74ACT11646
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

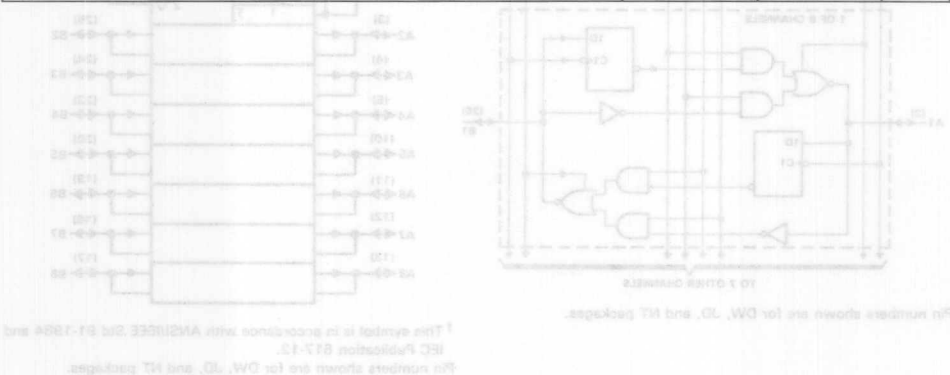
Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11646		74ACT11646		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		-24		-24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C



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Advanced CMOS Circuits

PRODUCT PREVIEW

54ACT11646, 74ACT11646
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11646		74ACT11646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA [†]	5.5 V				1.65				
	I _{OL} = 75 mA [†]	5.5 V						1.65		
	I _{OZ}	V _O = V _{CC} or GND	5.5 V		±0.5		±10		±5	
	I _I	V _I = V _{CC} or GND	5.5 V		±0.1		±1		±1	
	I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		8		160		80	
	ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V		0.9		1		1	
C _i	V _I = V _{CC} or GND	5 V		4						pF
C _o	V _O = V _{CC} or GND	5 V		10						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements, V_{CC} = 5 ± 0.5 V (see Figure 1)

		T _A = 25°C		54ACT11646		74ACT11646		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency							MHz
t _w	Pulse duration, CAB or CBA high or low							ns
t _{su}	Setup time, A before CLK [†] or B before CBA [†]							ns
t _h	Hold time, A after CAB [†] or B after CBA [†]							ns

54ACT11646, 74ACT11646
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} RANGE	T _A = 25°C			54ACT11646		74ACT11646		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			5.0 ± 0.5 V								MHz
t _{PLH}	A or B	B or A	5.0 ± 0.5 V		5.1						ns
t _{PHL}					7.2						
t _{PZH}	\bar{G}	A or B	5.0 ± 0.5 V		6.2						ns
t _{PZL}					7.2						
t _{PHZ}	\bar{G}	A or B	5.0 ± 0.5 V		6.5						ns
t _{PLZ}					7.2						
t _{PLH}	CBA or CAB	A or B	5.0 ± 0.5 V		6.4						ns
t _{PHL}					9						
t _{PZH}	DIR	A or B	5.0 ± 0.5 V		7						ns
t _{PZL}					8						
t _{PHZ}	DIR	A or B	5.0 ± 0.5 V		6.6						ns
t _{PLZ}					7.3						
t _{PLH}	SBA OR SAB (A or B high)	A or B	5.0 ± 0.5 V		6.1						ns
t _{PHL}					8.3						
t _{PLH}	SBA or SAB (A or B low)	A or B	5.0 ± 0.5 V		6.1						ns
t _{PHL}					8.3						

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C _L = 50 pF, f = 1 MHz	45	pF
		Outputs disabled		12	

UNIT	54ACT11646		74ACT11646		T _A = 25°C	
	MIN	MAX	MIN	MAX	MIN	MAX
ns						
ns						
ns						
ns						

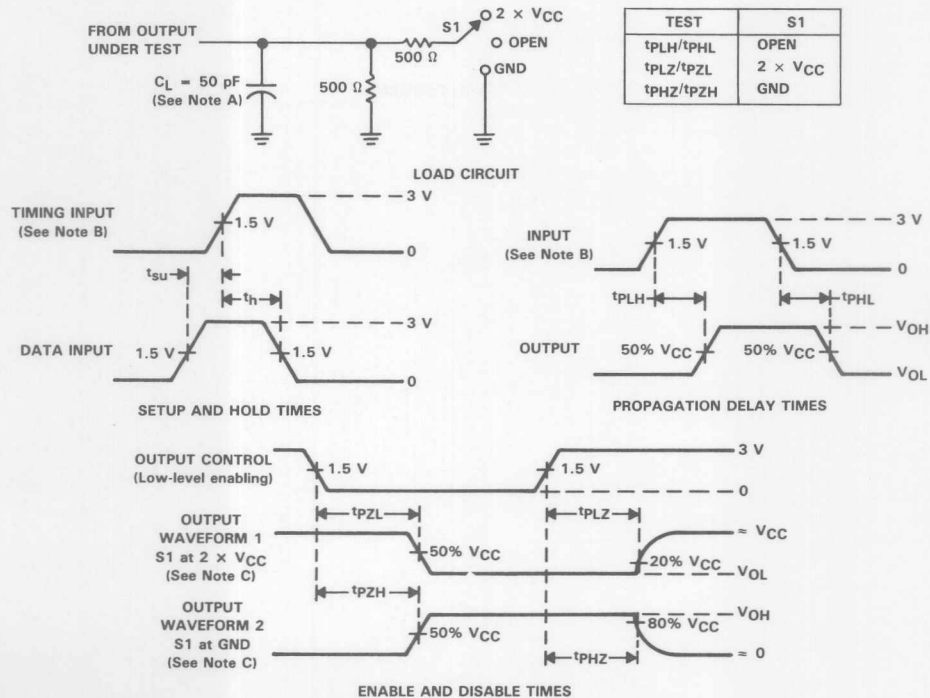
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Advanced CMOS Circuits

PRODUCT PREVIEW

54ACT11646, 74ACT11646
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION

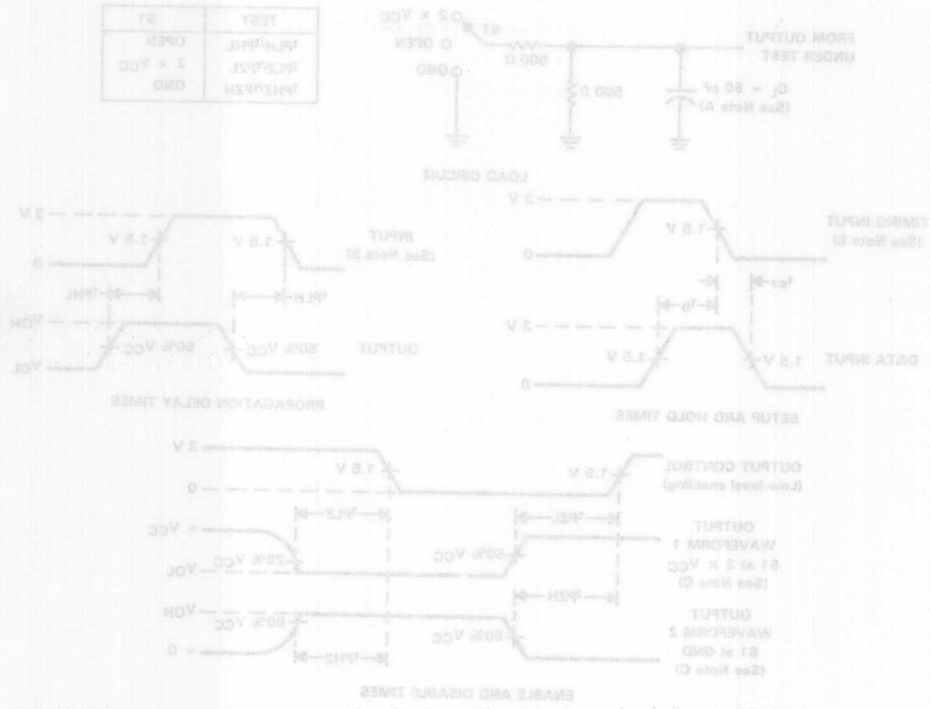


- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

NOTE: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generator having the following characteristics: $PRR \leq 10 \text{ MHz}$, $V_H = 3.0 \text{ V}$, $V_L = 0 \text{ V}$, $t_r = 3 \text{ ns}$.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.



PARAMETER MEASUREMENT INFORMATION

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

8A0CT11848, 7A0CT11848

General Information

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Glossary
Explanation of Function Tables
D Flip-Flop and Latch Signal Conventions
Thermal Information
Parameter Measurement Information
Functional Index
Device Pin-Outs

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Mechanical Data

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Ordering Instructions
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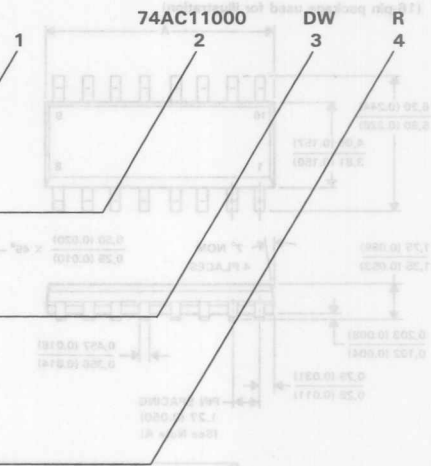
ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

EXAMPLE

1. **Prefix** _____
Blank = Standard product
SNJ = JEDEC Publication 101, Class B
JANB = MIL-M-38510 Qualified
2. **Unique Circuit Description** _____
Must contain 9 or 10 characters
(From individual data sheet)
3. **Package** _____
Must contain one or two letters
J, JD, JT, N, NT
D, DW ("Small Outline" Packages)
FK (Leadless Ceramic Chip Carrier)
4. **Tape and Reel Packaging** _____
Must be designated by the letter R and valid for surface mount packages only.
All orders for tape and reel must be for whole reels.

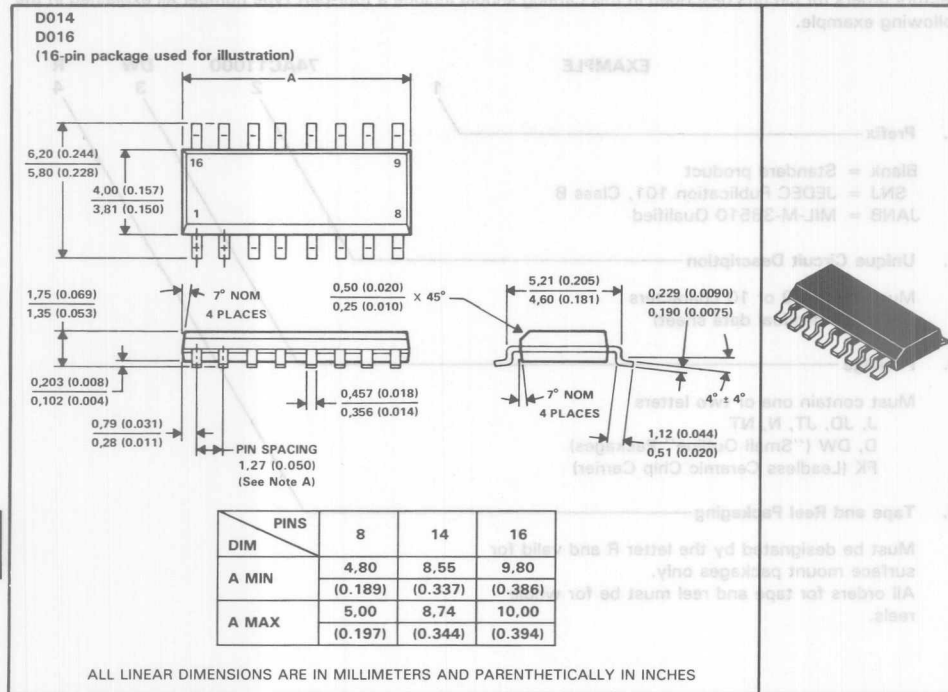


valid for	95.2	95.2	95.2
whole	95.2	95.2	95.2

MECHANICAL DATA

D014 and D016 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

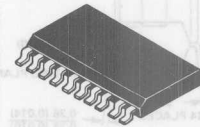
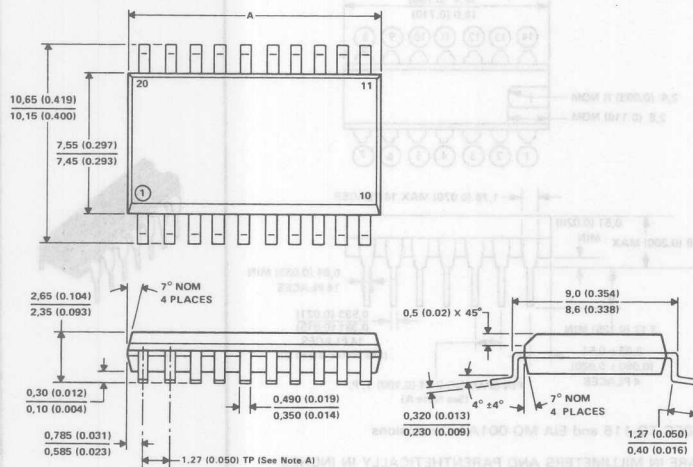


- NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within $\pm 0,051$ (0.002) exclusive of solder.

DW020, DW024, and DW028 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DW020
DW024
DW028
(20-pin package used for illustration)



	PINS	16	20	24	28†
DIM					
A MIN		10.16 (0.400)	12.70 (0.500)	15.29 (0.602)	17.68 (0.696)
A MAX		10.36 (0.408)	12.90 (0.508)	15.49 (0.610)	17.88 (0.707)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

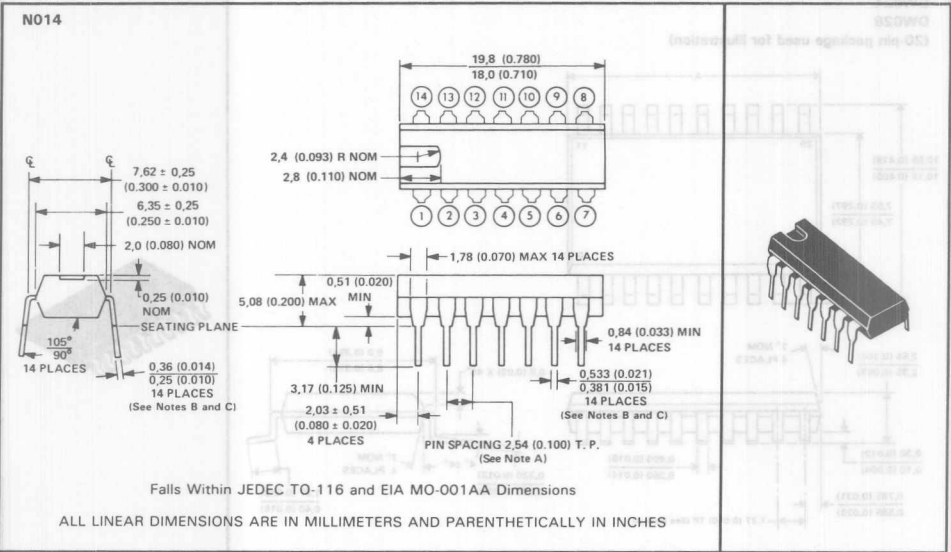
†The 28-pin package drawing is presently classified as Advance Information.

- NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within $\pm 0,051$ (0.002) exclusive of solder.

MECHANICAL DATA

N014 plastic dual-in-line package

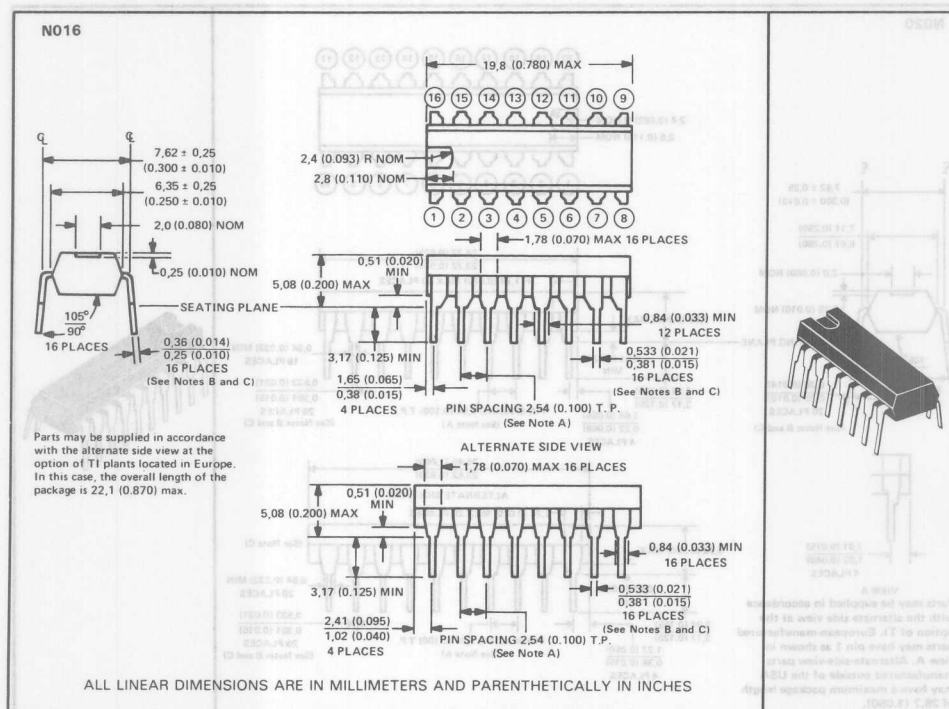
This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.51 (0.020) above seating plane.

N016 plastic dual-in-line package

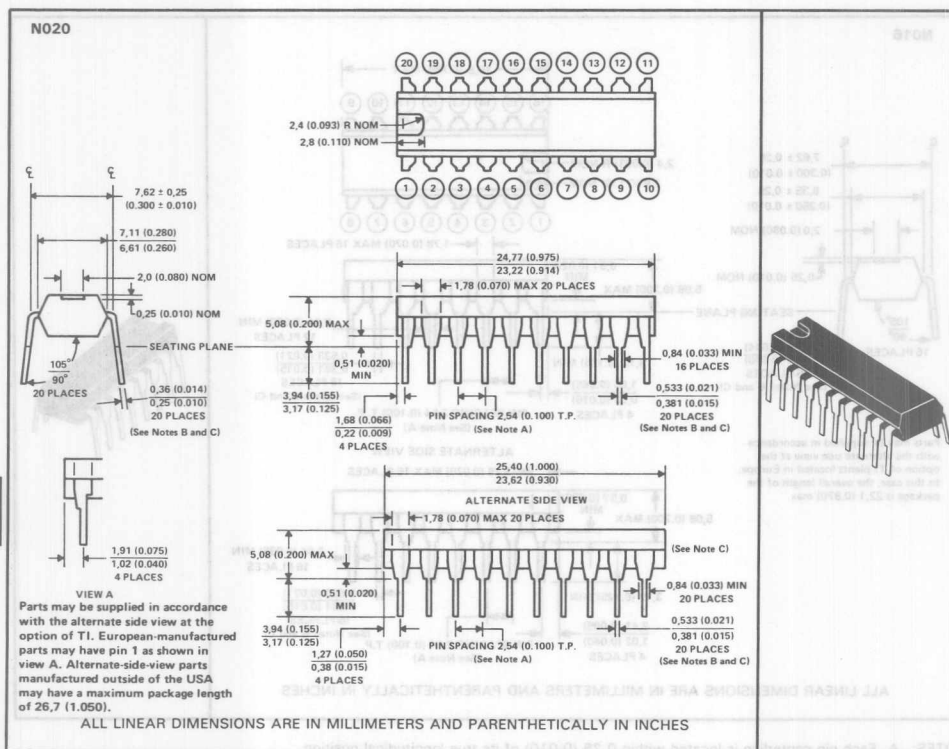
This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



MECHANICAL DATA

N020 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

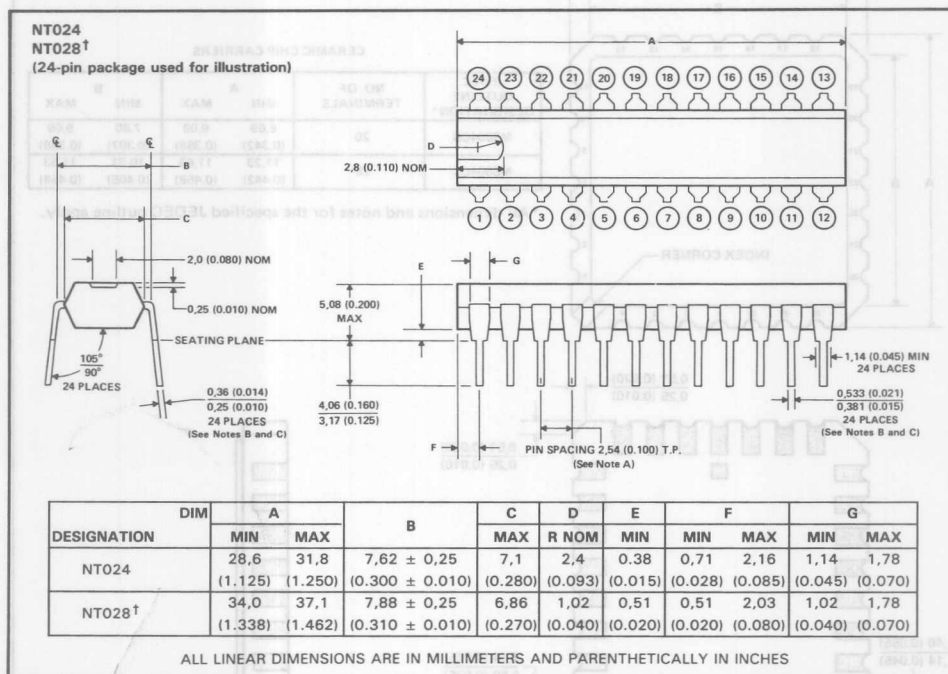


- NOTES:
- Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
 - This dimension does not apply for solder-dipped leads.
 - When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NT024 and NT028† plastic dual-in-line packages

Each of these packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin and 28-pin packages, the letter N is used by itself since the 24-pin and 28-pin packages may be available in more than one row-spacing. For the 24-pin and 28-pin packages, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.



† The 28-pin package drawing is presently classified as Advance Information.

NOTES: A. Each pin centerline is located within 0.25 mm (0.010 inch) of its true longitudinal position.

B. This dimension does not apply for solder-dipped leads.

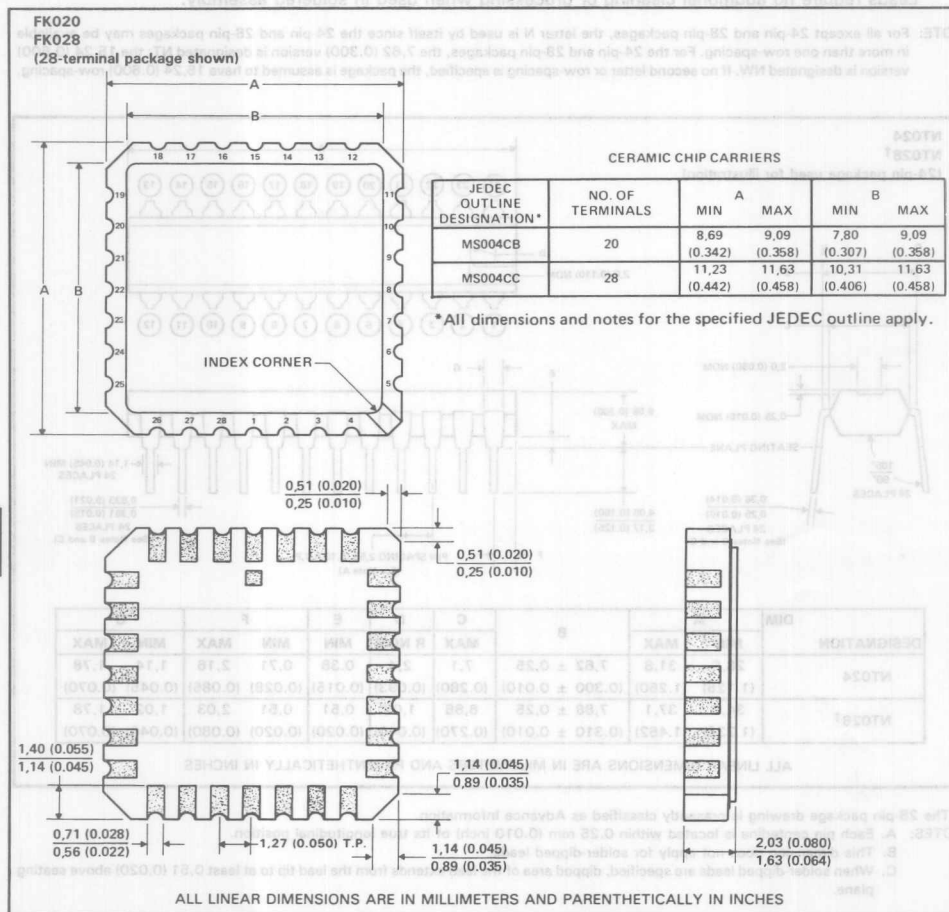
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

MECHANICAL DATA

FK020 and FK028 ceramic chip carrier packages

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.

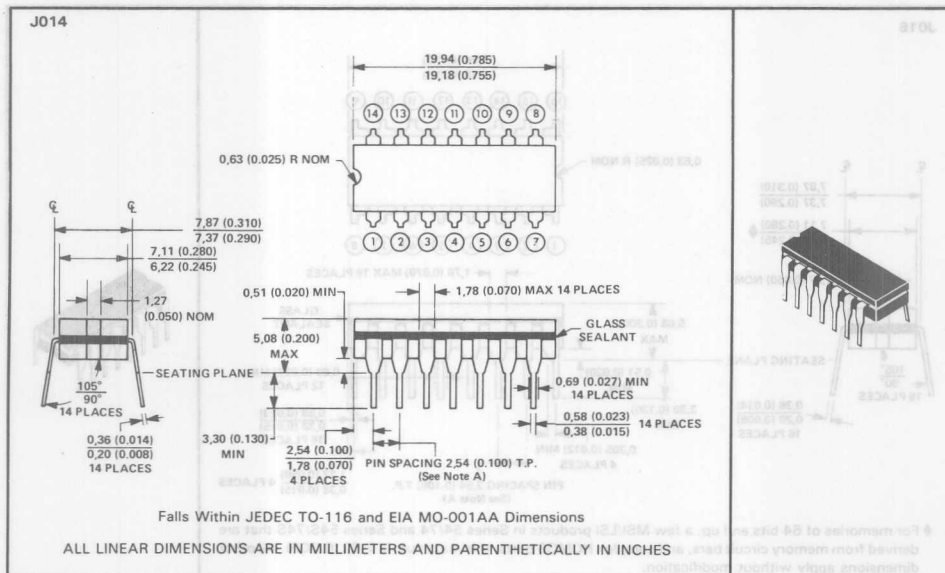


3

Mechanical Data

J014 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

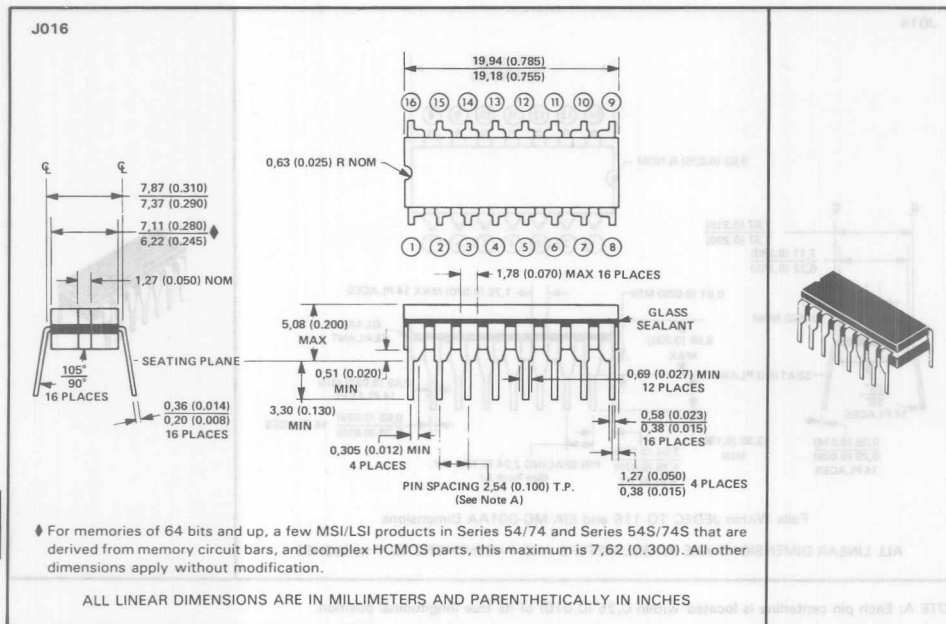


NOTE A: Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.

MECHANICAL DATA

J016 ceramic dual-in-line package

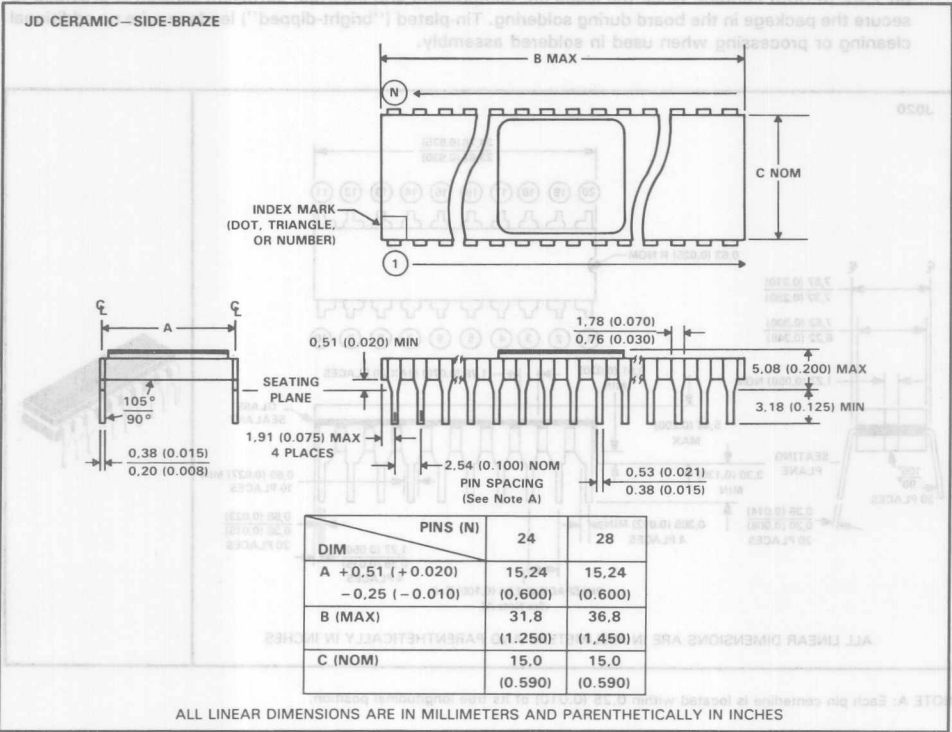
This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



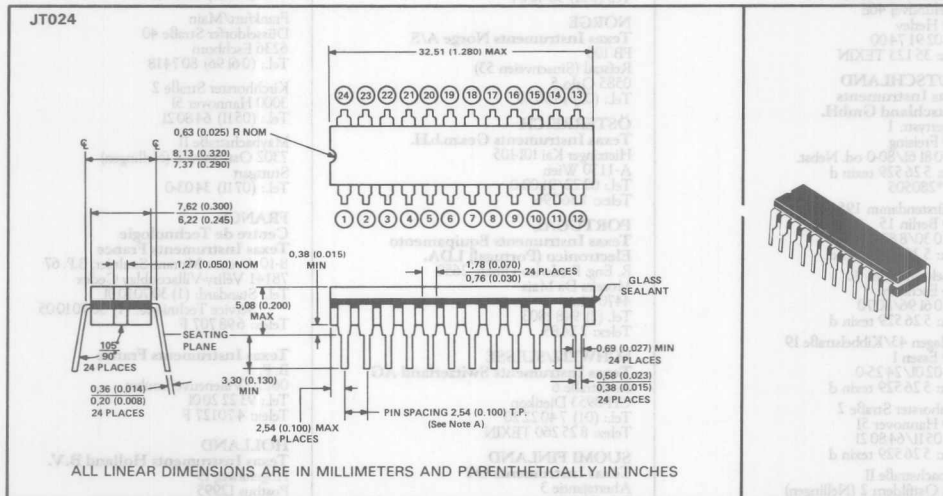
MECHANICAL DATA

JD ceramic side-braze dual-in-line packages

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.



This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the pins are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") pins require no additional cleaning or processing when used in soldered assembly.



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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